A High-Density Subthreshold SRAM with Data-Independent Bitline Leakage and Virtual Ground Replica Scheme

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Agenda

- Introduction to Subthreshold Operation
- Proposed Subthreshold SRAM
  - Decoupled 10T SRAM Cell
  - Write margin improvement utilizing Reverse Short Channel Effect (RSCE)
  - Data-independent bitline leakage
  - Virtual ground replica scheme
  - Write-back scheme for stability
- 0.2V 480kb SRAM Measurements
- Conclusions

Introduction to Subthreshold Operation

- **Characteristics**
  - V_{GS} is smaller than V_{TH}
  - Exponential current equation

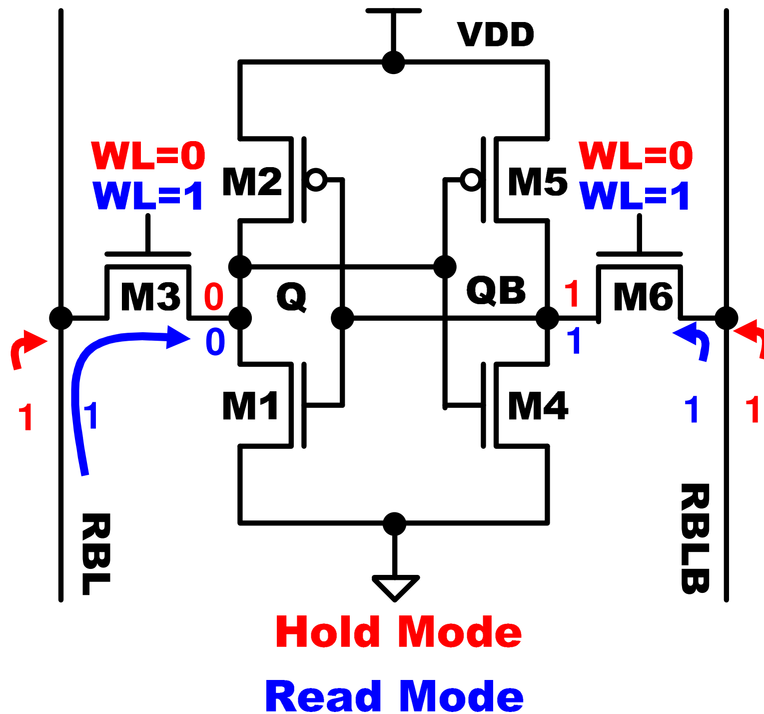
$$I_D = I_{D0} \frac{W}{L_{eff}} e^{\frac{V_{GS} - V_{th}}{mV_t}} (1 - e^{\frac{-V_{DS}}{V_t}})$$

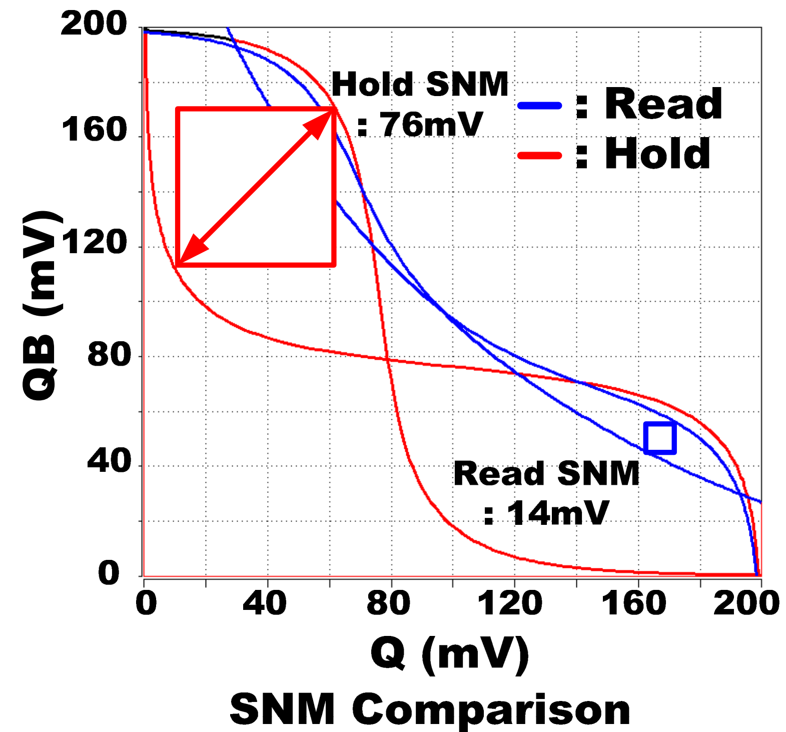
  - For low power, minimum energy applications
- **Applications of Subthreshold SRAM**
  - Wireless sensor nodes: data memory for DSPs
  - Medical devices: hearing aids, pacemakers
  - Portable electronics: cellular phones, PDAs

Subthreshold SRAM Design Issues

- Mainly due to small I_{on}-to-I_{off} ratio and current variation in subthreshold
  - Read failure
    : Reduced SNM, small bitline sensing margin
  - Write failure
    : Weak write path
  - Limited array efficiency
    : Data-dependent bitline leakage
  - Performance and power variation

SNM of 6T SRAM Cell

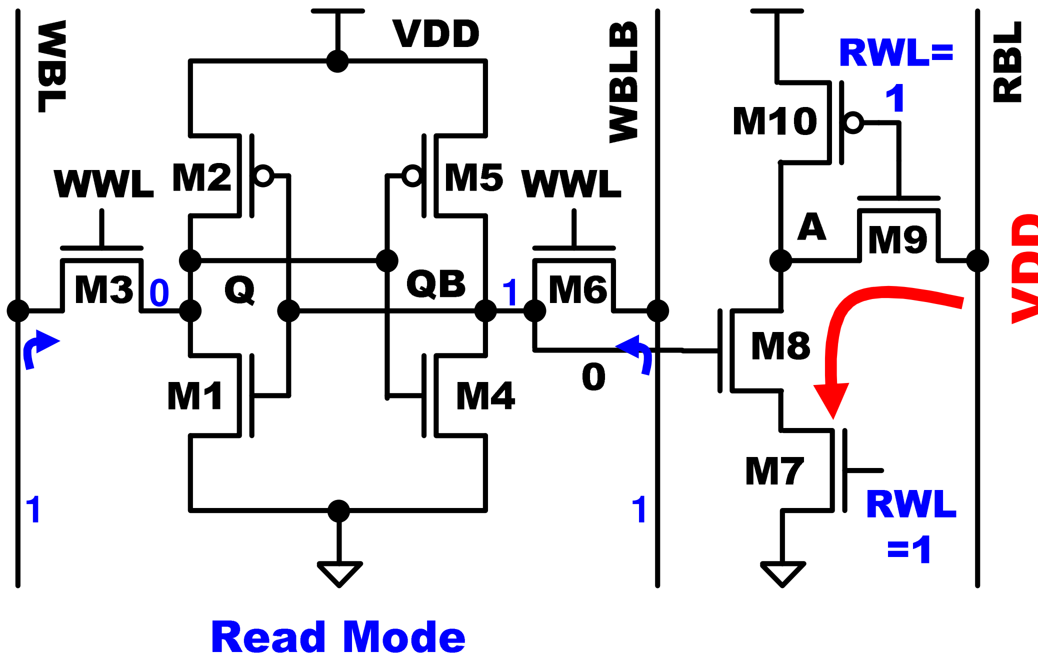


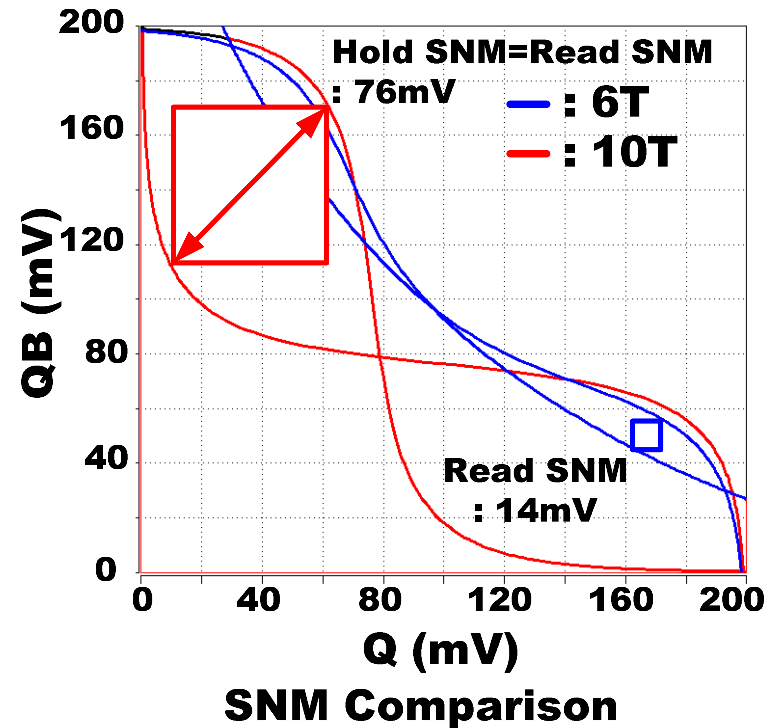


SNM Comparison

- Read SNM is 18% of hold SNM at 0.2V
- Read SNM is too small for robust subthreshold operation

SNM of Proposed 10T SRAM Cell

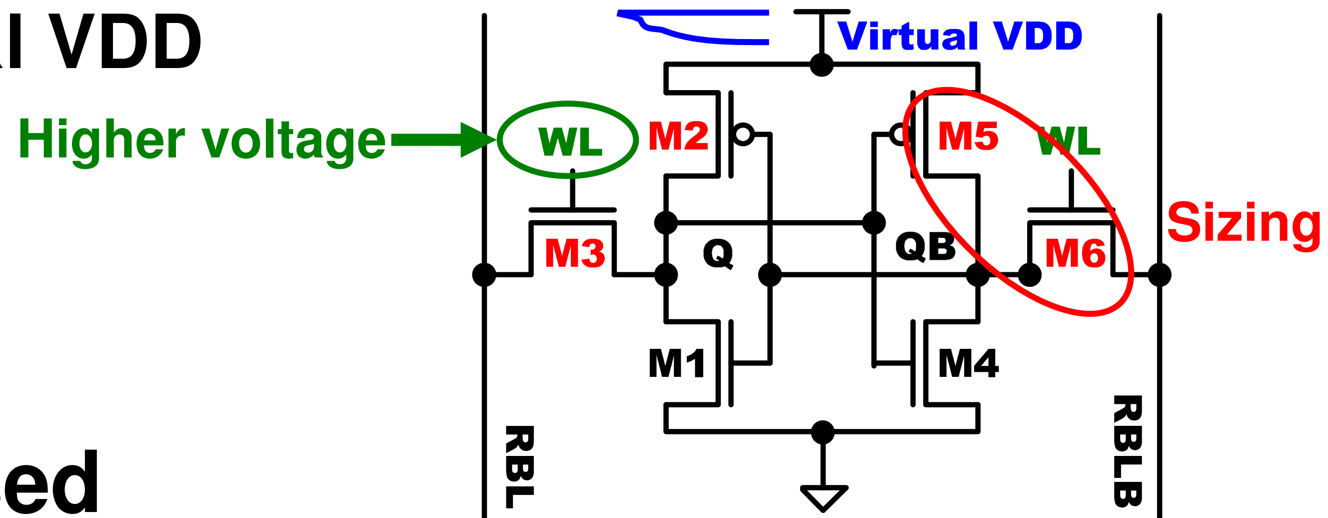




- Decoupled cell node
- Read SNM is equal to hold SNM
- SNM = 38% of supply voltage
- Stability only limited by cross-coupled latch

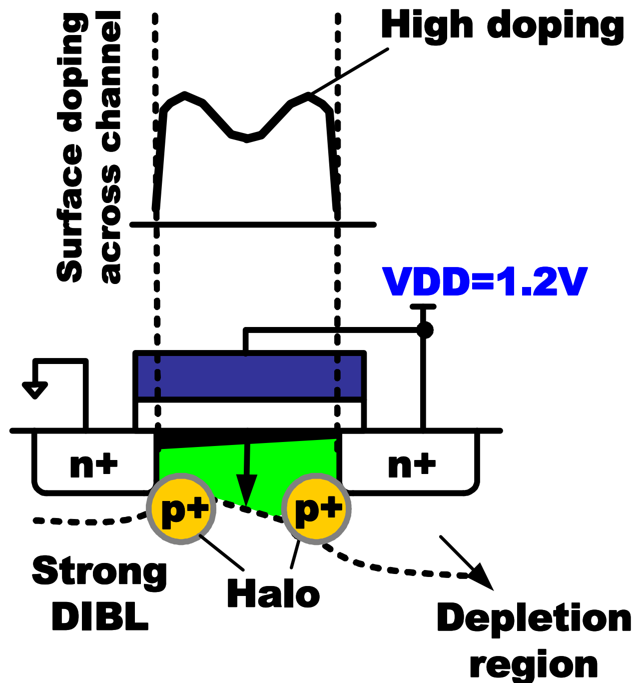
Write Margin Improvement

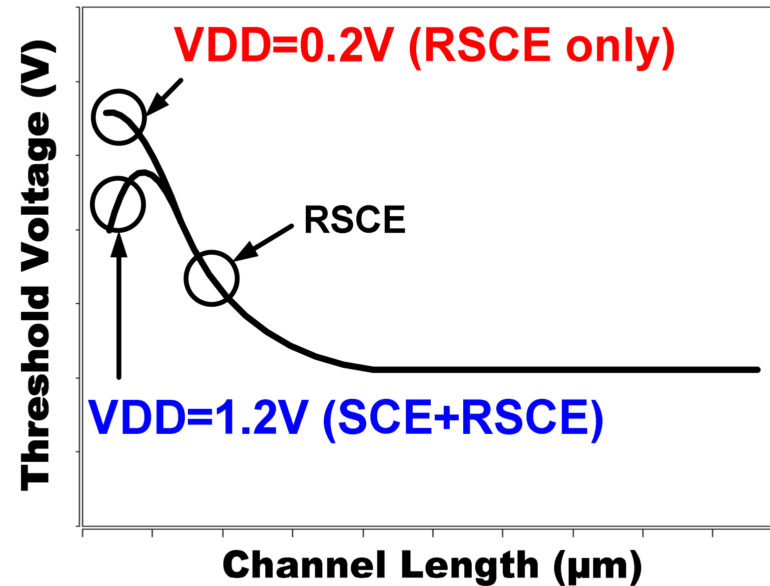
- Conventional Techniques
  - Sizing: access TR vs. PMOS in latch
  - Higher WL voltage for access TR
  - Virtual VDD

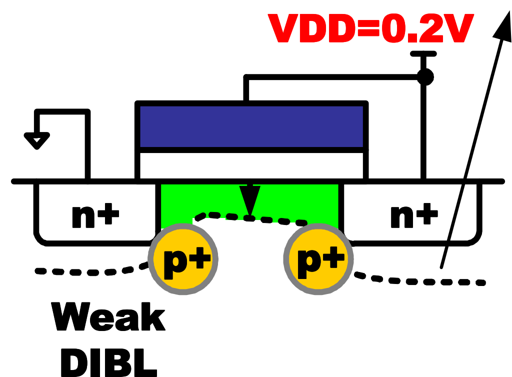


- Proposed
  - Utilize Reverse Short Channel Effect (RSCE) to strengthen write path

HALO Impact in Subthreshold

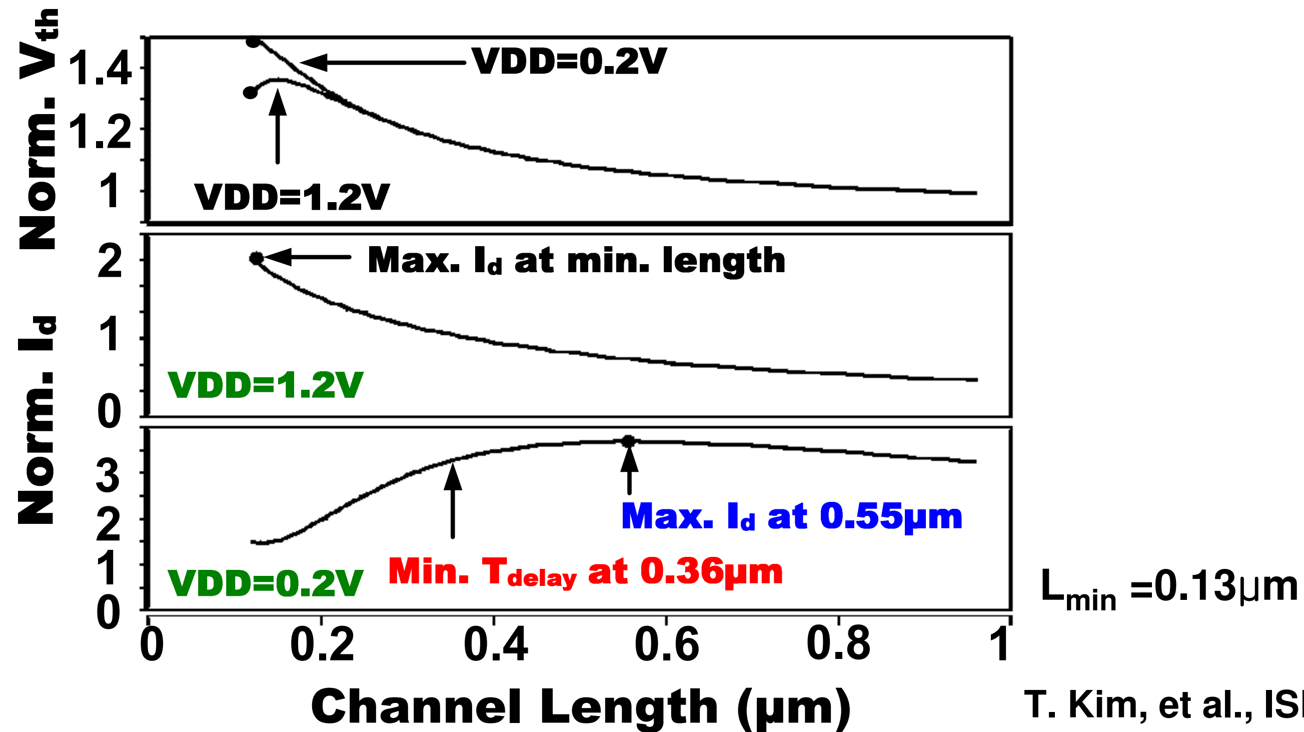






- **HALO to mitigate Short Channel Effect (SCE) in superthreshold**
- **Negligible SCE in subthreshold region**
- **Dominant RSCE in subthreshold region**

Utilizing RSCE for Improved Drive Current



L_{min} =0.13µm

T. Kim, et al., ISLPED06

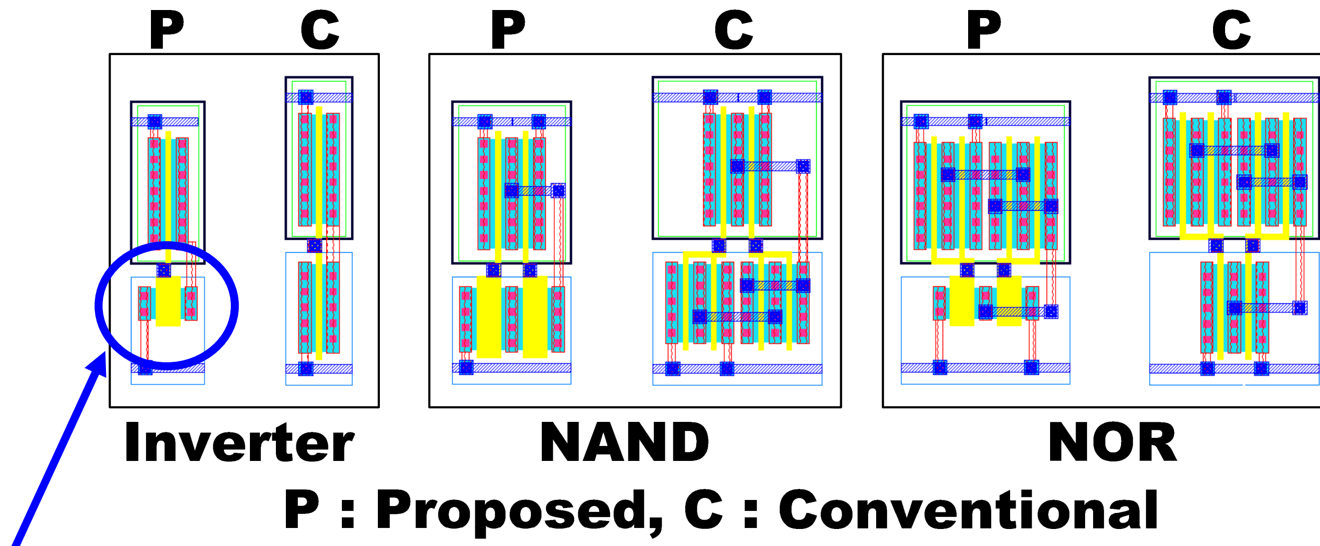
- Optimal channel length in subthreshold region
  - L_{opt}=0.55µm for max. current/width
  - L_{opt}=0.36µm for max. performance/width

Utilizing RSCE for Write Margin Improvement

TR utilizing RSCE
Additional 8.5% area increase

- Write access TRs utilizing RSCE ($L=3xL_{min}$)
- Increased current drivability: 3.3x at 0.2V
- Write margin improvement of 70mV at 0.2V

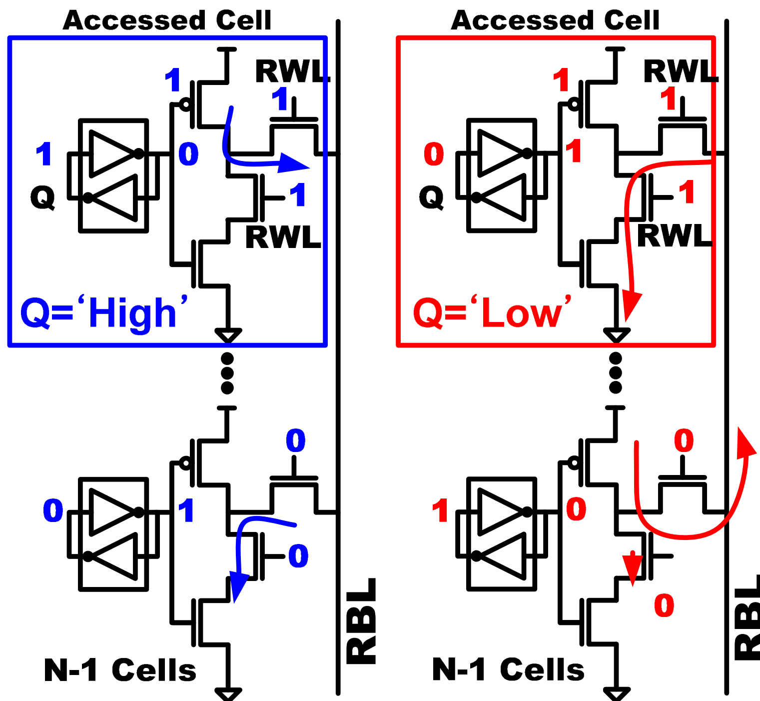
Utilizing RSCE for Delay Improvement

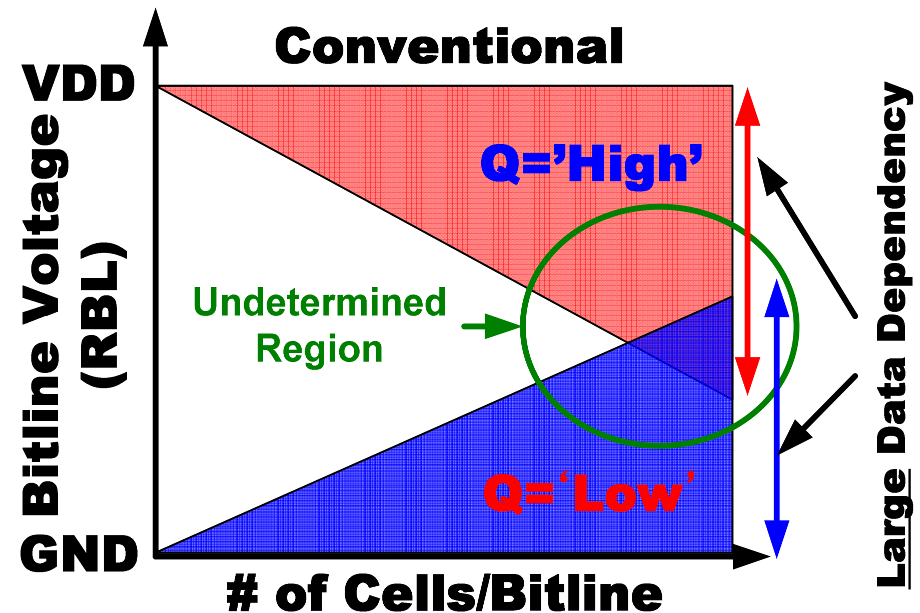


Fat NMOS devices to utilize RSCE

- Narrower width for the same current drivability
- Reduced junction capacitance
- Improved delay due to reduced capacitance

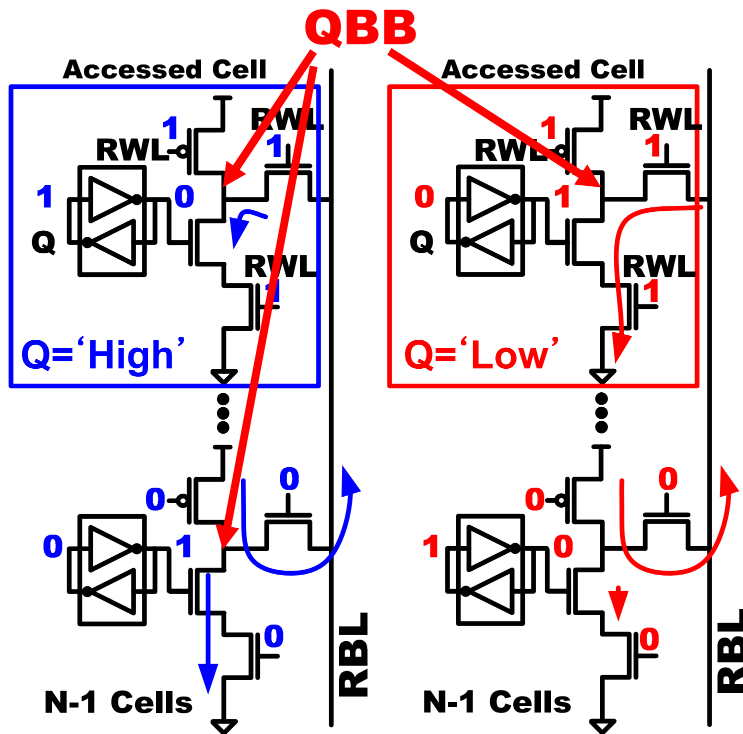
Data-Dependent BL Leakage Problem

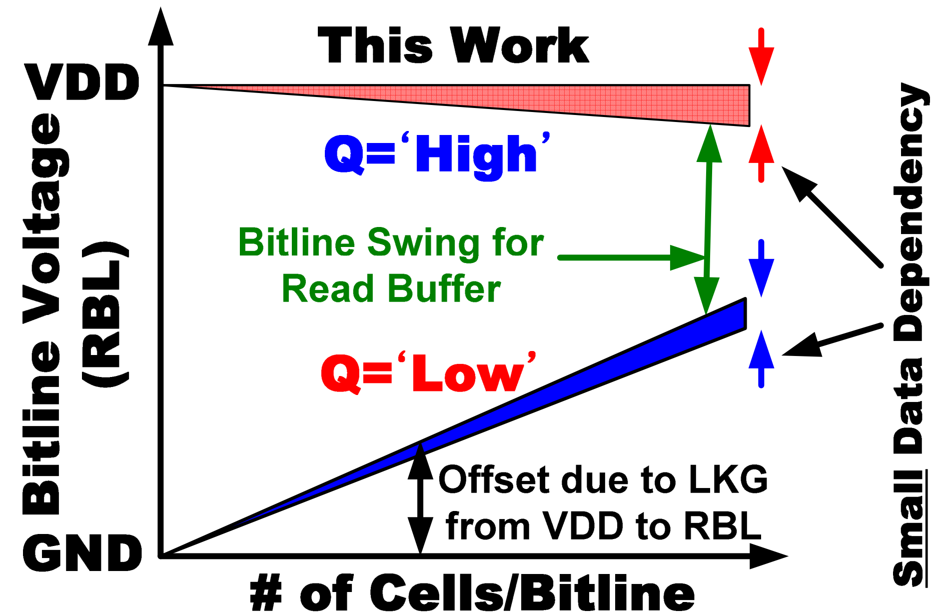




- Undetermined region due to data-dependency
- Possible read failure using single threshold read buffer

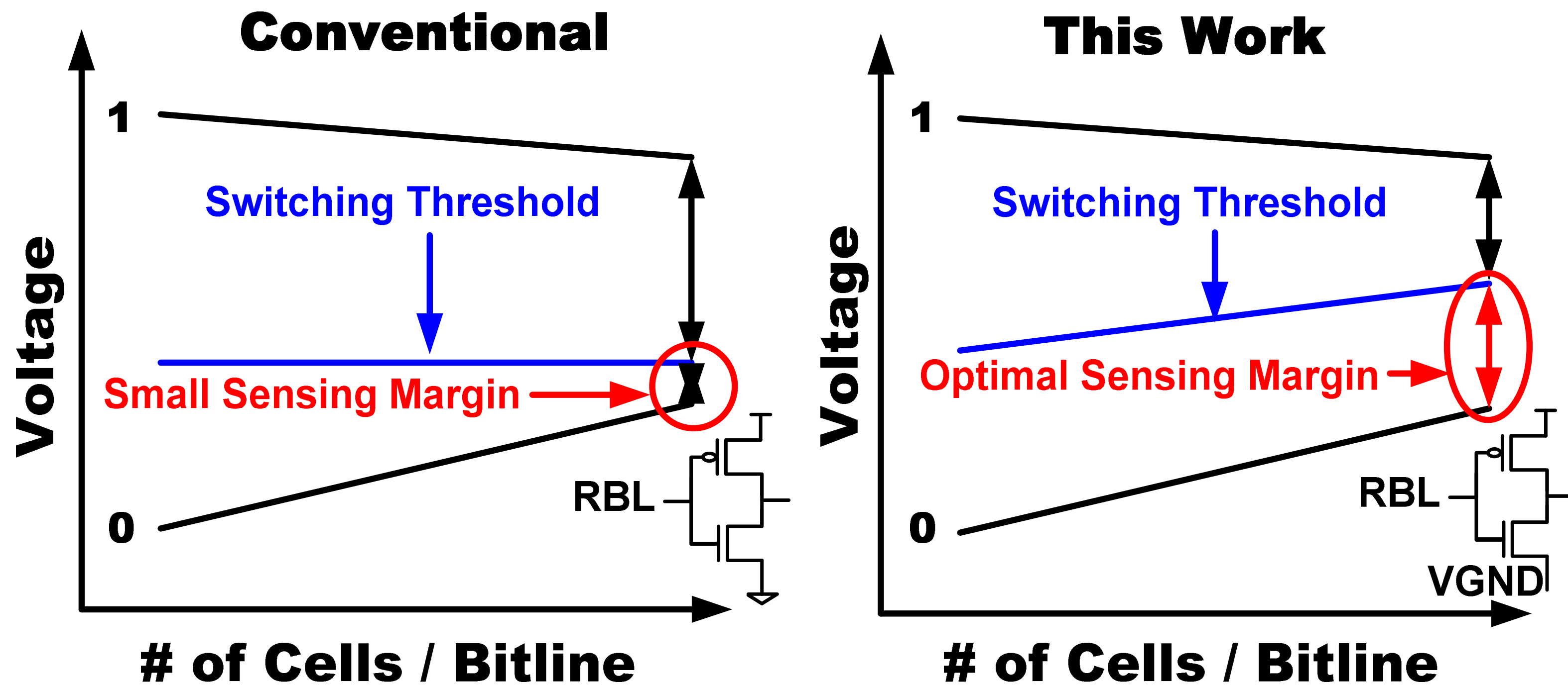
Proposed Scheme with Data-Independent BL Leakage





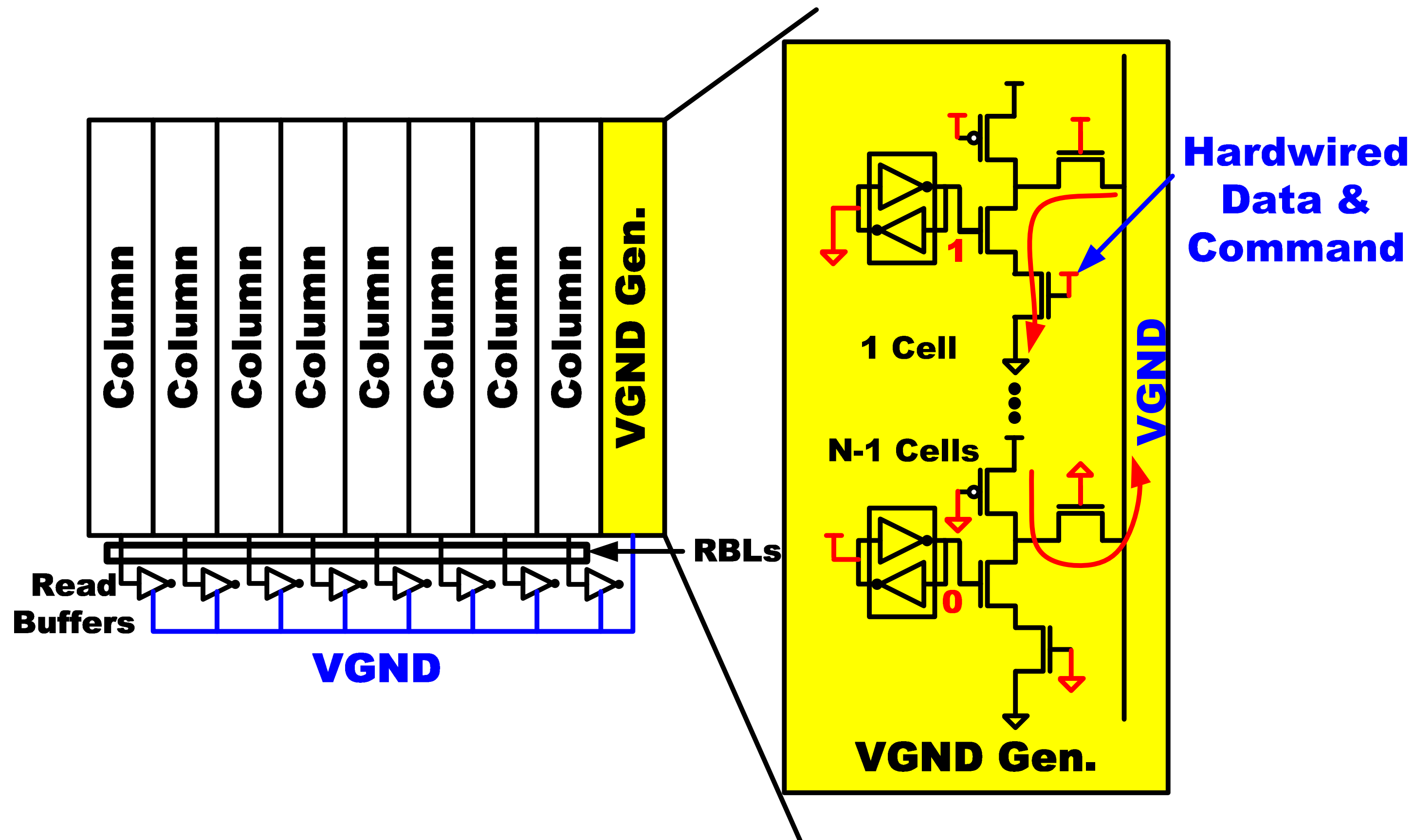
- Bitline logic high and low levels are fixed
- Logic level difference of 130mV at 0.2V with 1kcells/bitline

Virtual Ground Replica Scheme



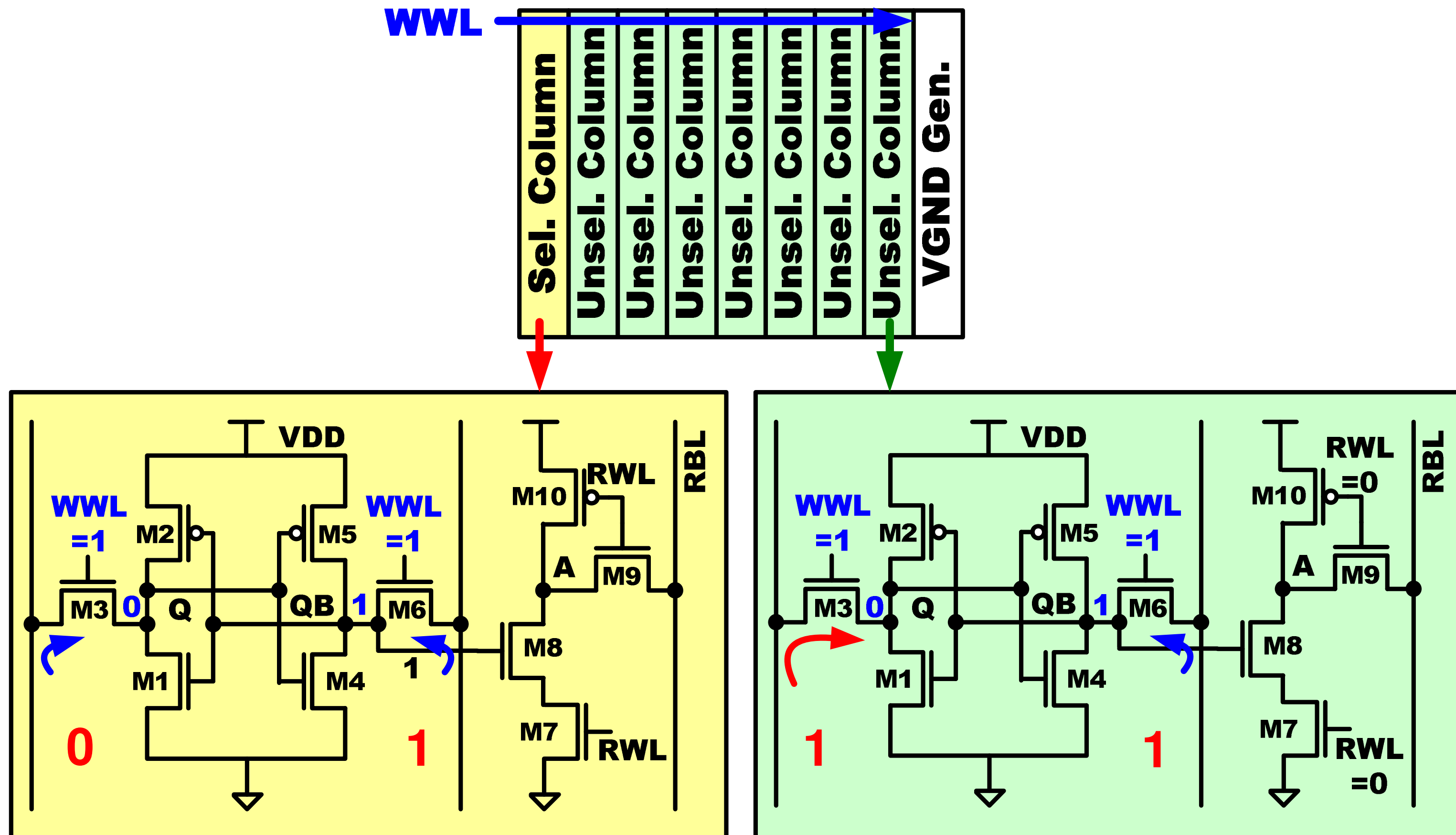
- Conventional: fixed switching threshold
- This work: VGND tracks RBL logic low level

Virtual Ground Replica Scheme



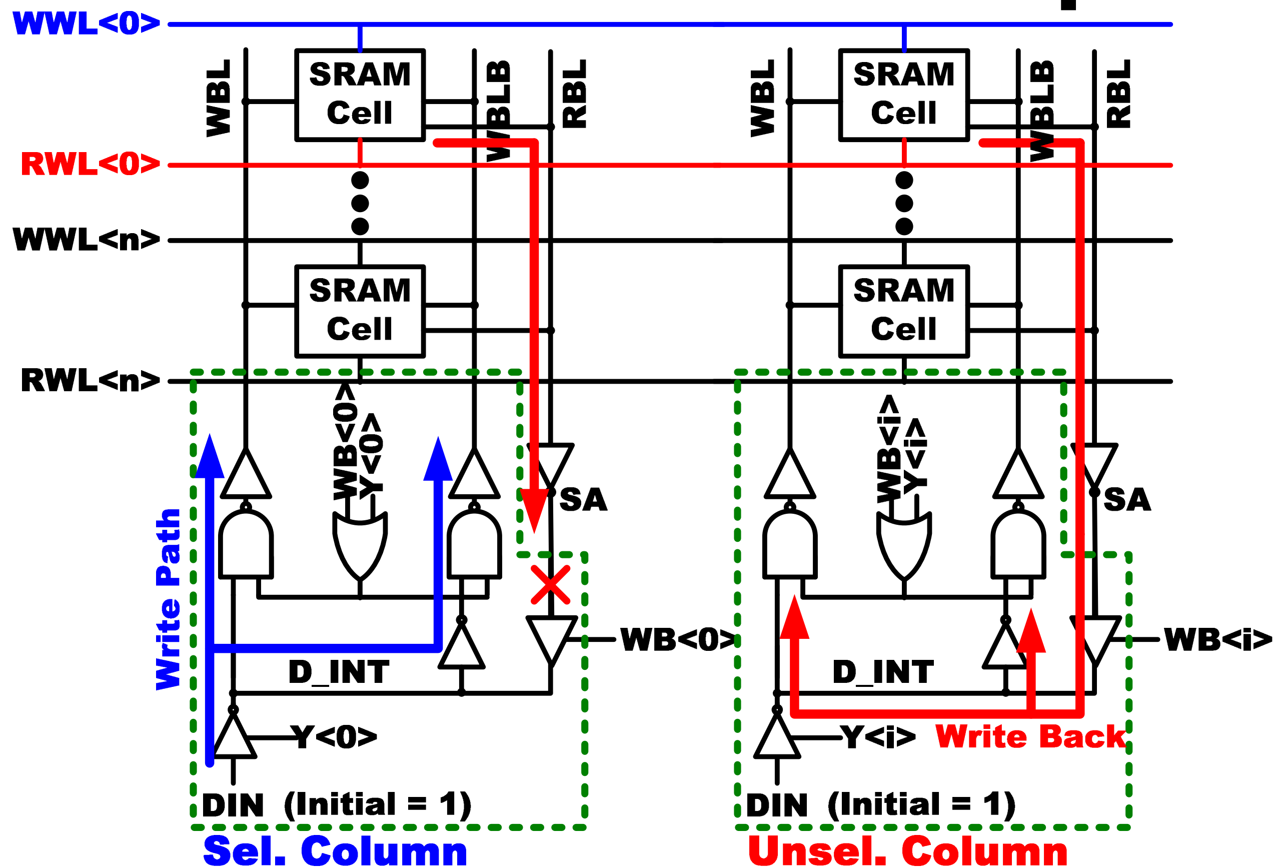
- Shared VGND across multiple read buffers
- Replica bitline with fixed data to generate VGND

Pseudo-Write Problem



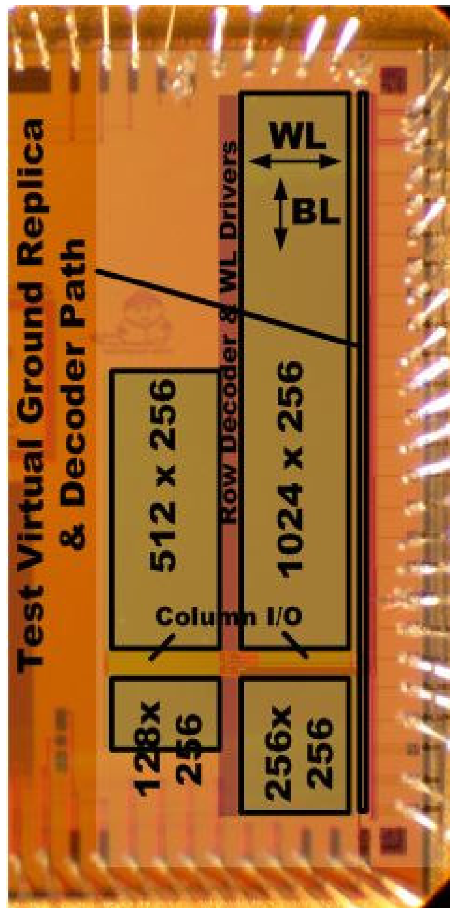
- Pseudo-write problem in unselected columns
- Worst case SNM due to current path

Write-Back Technique



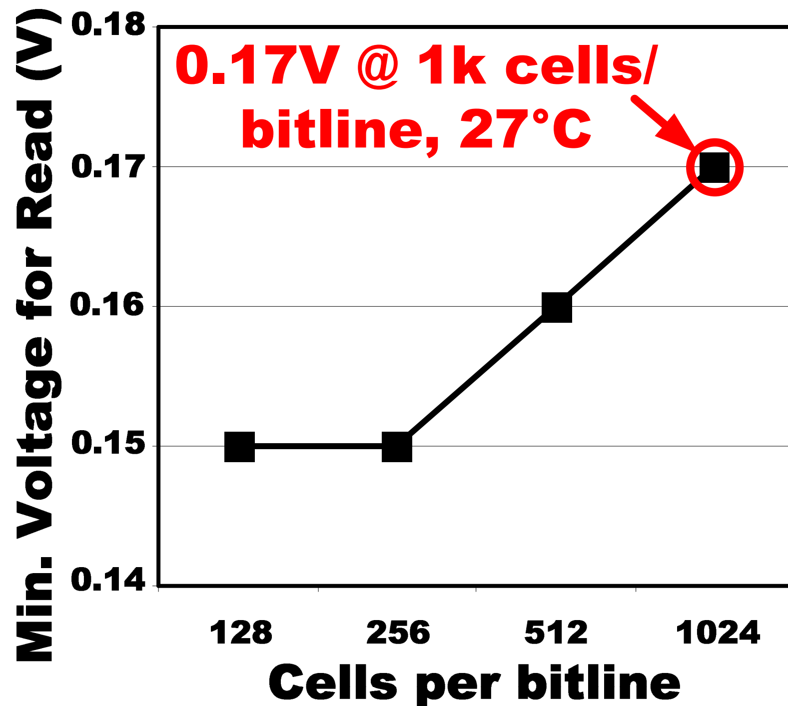
- Write after read to solve pseudo-write problem
- Write-back to unselected columns

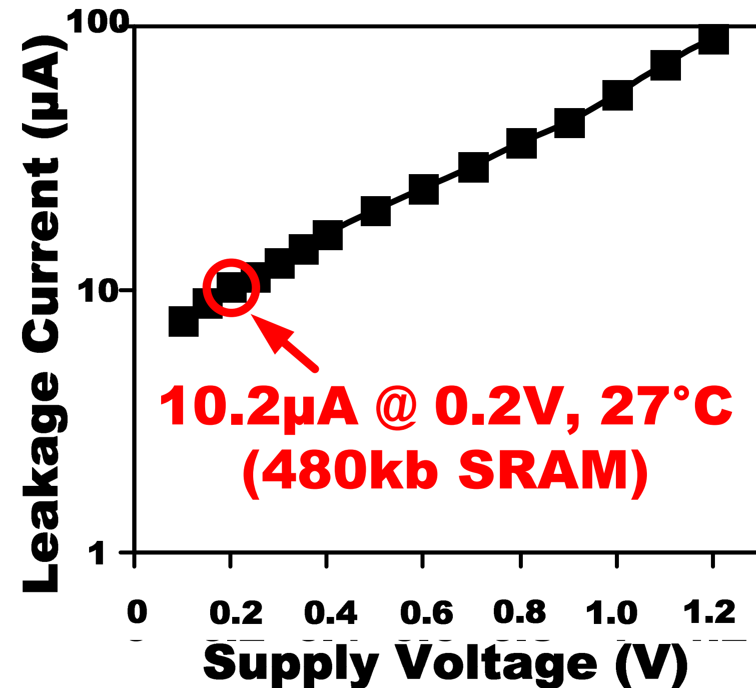
480kb SRAM Chip Implementation



Technology	130nm 8-metal CMOS
Chip Size	$4.1 \times 1.5 mm^2$
VCC min	0.2V @ 1024 Cells per Bitline, 27°C
Read Access Cycle	120kHz @ 0.2V, 27°C
Leakage Current (480k SRAM)	10.2μA @ 0.2V, 27°C
Read Bitline Swing	~0.1V @ 0.2V, 27°C

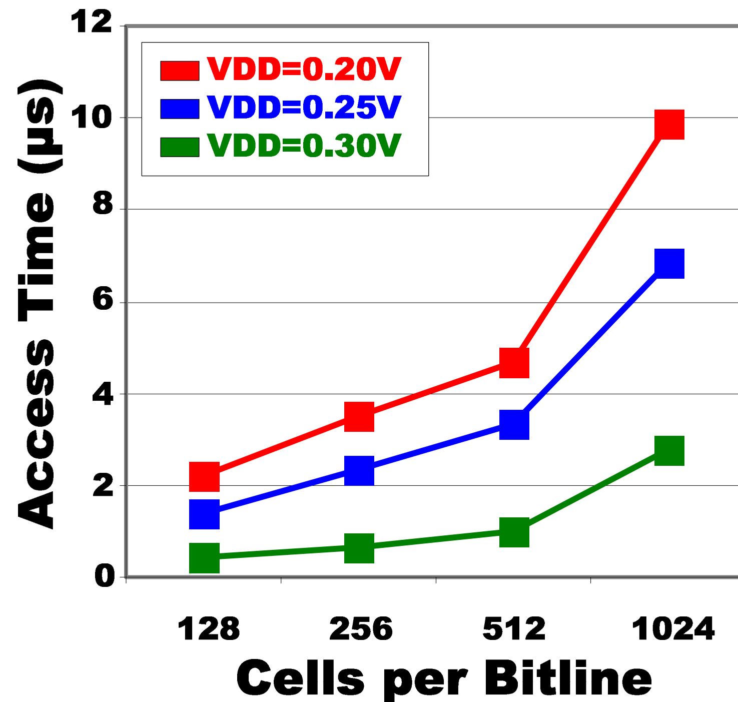
V_{min} and Leakage Measurements

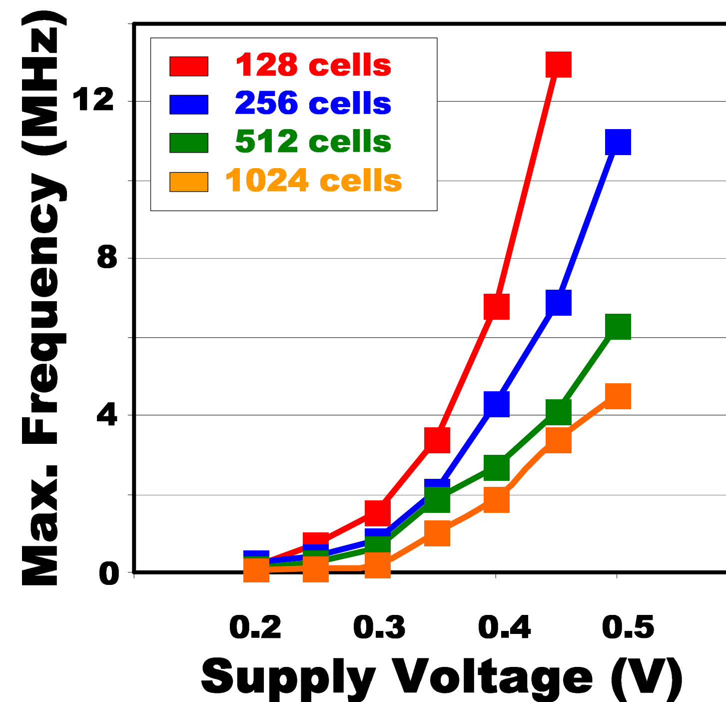




- V_{min_read} = 0.17V @ 1k cells/bitline
- V_{min_write} = 0.20V
- 90% I_{leak} reduction at 0.2V compared to 1.2V

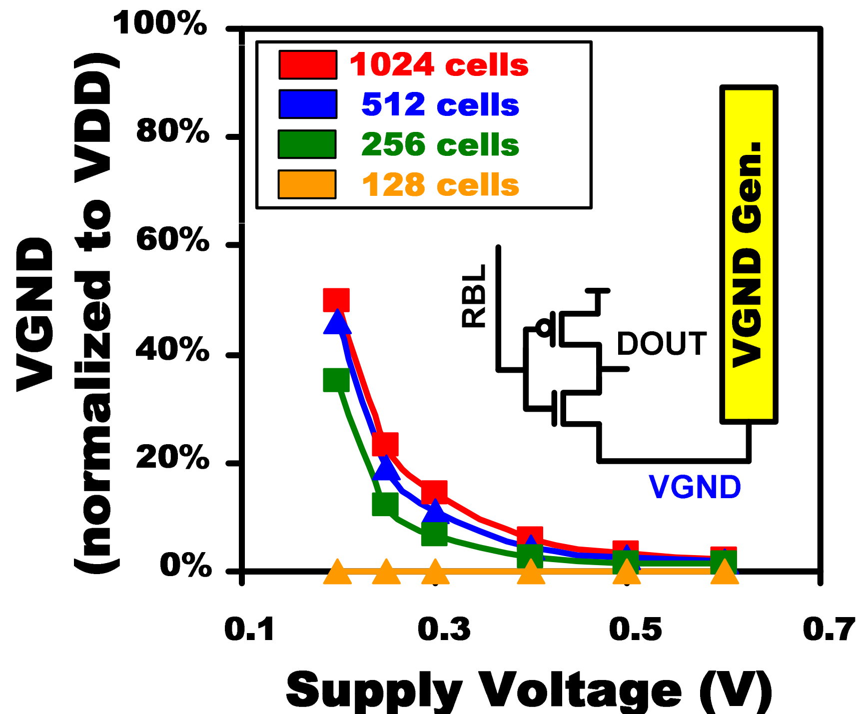
Performance Measurements

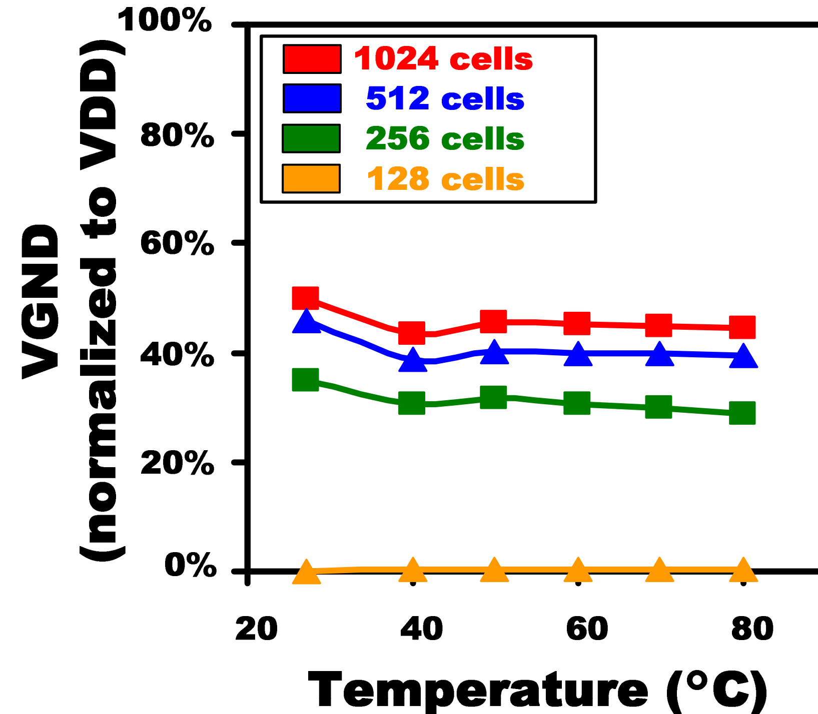




- 4.5x delay difference between four quadrants
- Exponential delay reduction with higher supply

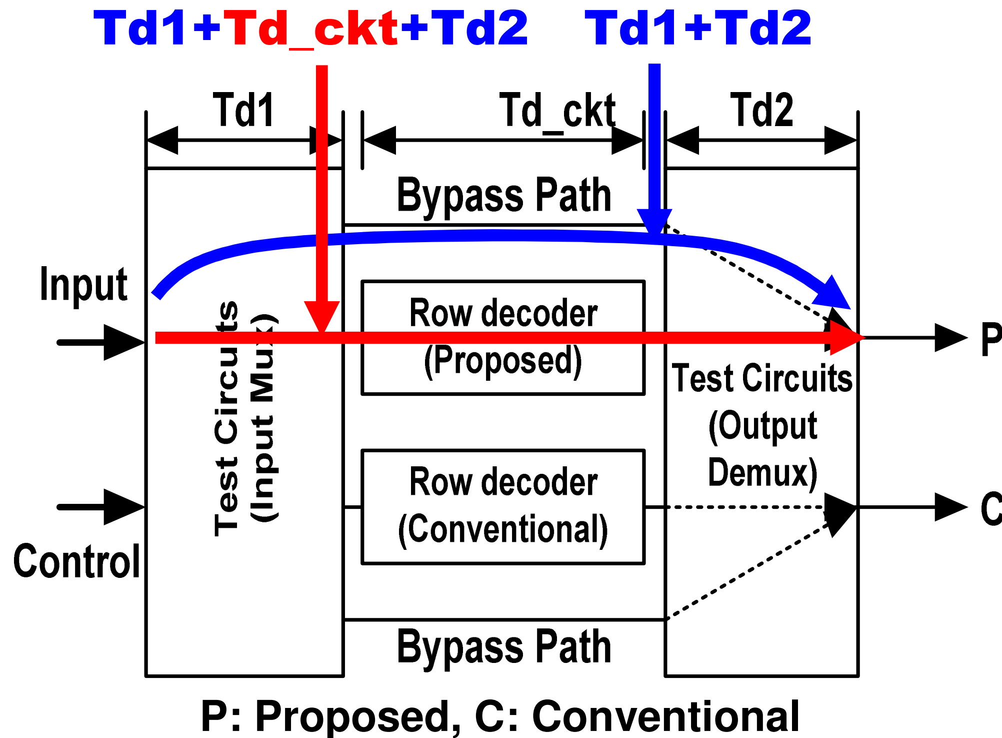
VGND Measurements



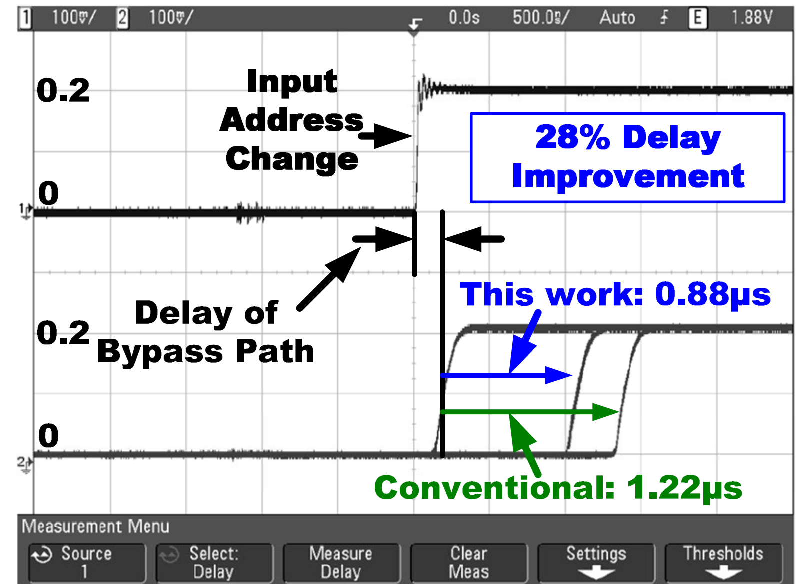


- Exponential increase of normalized VGND
- 0.1V bitline swing at VDD=0.2V
- VGND relatively constant with temperature

Improved Delay Utilizing RSCE



P: Proposed, C: Conventional



- Differential delay measurement circuit
- 28% delay improvement in predecoder utilizing RSCE

Conclusions

- Circuit techniques proposed to enable a 0.2V 480kb subthreshold SRAM
  - Decoupled 10T cell for improved read stability
  - Utilization of RSCE for improved write margin
  - Data-independent leakage for enabling 1k cells/bitline
  - Virtual ground replica scheme for optimal read buffer sensing margin
  - Write-back scheme to eliminate pseudo-write problem