Silicon Odometer: An On-Chip Reliability Monitor for Measuring Frequency Degradation of Digital Circuits

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Abstract

A fully-digital reliability monitor is presented for high resolution frequency degradation measurements of digital circuits. The proposed scheme measures the beat frequency of two ring oscillators, one which is stressed and the other which is unstressed, to achieve 50X higher delay sensing resolution compared to prior techniques. A reliability monitor test chip has been fabricated in a 1.2V, 130nm CMOS technology.

Introduction

Bias Temperature Instability (BTI), Hot Carrier Injection (HCI), and Time Dependent Dielectric Breakdown (TDDB) have become major reliability concerns undermining the performance and yield of nanoscale VLSI systems. Accurate measurement of digital circuit reliability is imperative for designing systems tolerant to device aging. Previous reliability measurements relied on device probing or on-chip ring oscillators, which either require an extensive measurement setup or have limited sensing resolution [1,2]. Moreover, they were inefficient in collecting large population data under various stress conditions, which is crucial in understanding further complex behavior of aging (e.g. statistical behavior, process dependency, frequency dependency). This paper describes a fully-digital on-chip reliability monitor for accurately measuring frequency degradation induced by device stress. Our proposed technique achieves 50X higher frequency sensing resolution than prior techniques by detecting the beat frequency between a stressed ring oscillator and an unstressed ring oscillator. Various stress modes and on-chip configuration facilitate data acquisition for studying complex device aging behavior. A 265x132μm^2 test chip was fabricated in a 1.2V, 130nm CMOS process to demonstrate the proposed reliability monitor concept.

Proposed Reliability Monitor Circuit

The core circuit for detecting frequency degradation consists of two free-running ring oscillators and a phase comparator as shown in Fig. 1. One of the ring oscillators is stressed and the other is unstressed. The supply voltage of the stressed ring oscillator is raised to $V_{DD\text{-}STR}$ during stress periods and lowered to $V_{DD\text{-}NOM}$ during the periodic measurements. The supply voltage of the reference ring oscillator is lowered to 0V during the stress periods to prevent device aging and periodically raised to $V_{DD\text{-}NOM}$ for the measurements. The output of the phase comparator exhibits the beat frequency f_{stress}-f_{ref}, where f_{stress} is the stressed ring oscillator frequency and f_{ref} is the reference ring oscillator frequency. A counter using the reference ring oscillator signal as the clock measures the beat frequency. The counter output N is measured after each stress period to calculate the percent frequency degradation according to the relationship in Fig. 2. Previous measurement techniques using a single stressed ring oscillator have limited sensing resolution as the counter output N is proportional to the frequency degradation. For example, 1% degradation in ring oscillator frequency translates into 1% change in counter output as displayed in Fig. 3. On the other hand, the counter output using our proposed scheme changes by 50% for the same amount of degradation offering an improved sensing resolution. Note that the resolution of the proposed reliability monitor (i.e. $\Delta N/\Delta f_{stress}$) depends on the initial counter output N that is set before the stress experiments. An initial N of 100 (or 256) allows a sensing resolution of 0.01% (or 0.0015%). The closer the frequencies of the two ring oscillators are brought together initially (i.e. the larger the initial N), the larger change in the counter output is observed for the same degradation in ring oscillator frequency. Measurement accuracy can be easily programmed by changing the initial counter output using delay trimming circuits.

Test Chip Implementation and Results

A system diagram of the reliability monitor fabricated in a 1.2V, 130nm CMOS is shown in Fig. 4. The two 105 stage ring oscillators are identical structures with different control inputs. Process-voltage-temperature (PVT) variations that affect both structures equally will not alter the monitor output as the affects will cancel out. Thick oxide I/O devices are used for the peripheral control circuits connected to the stress voltage. Bubbles (i.e. lone '1' in a stream of '0's or a '0' in a stream of '1's) that may appear in the phase comparator output due to jitter and other circuit uncertainties can be eliminated using a 5-bit majority voting circuit. The DETECT pulse generated by the beat frequency detector samples the counter output and resets the counter for the next measurement cycle. A parallel-to-serial register is used to scan out the measurement data. Fig. 5 shows a detail schematic of the ring oscillator with various stress mode controls. The virtual V_{DD} can be switched to $V_{DD\text{-}STRESS}$, $V_{DD\text{-}NOM}$, and 0V to allow for stress and measurement of the reference and stressed ring oscillators. Stress mode control #1 applies AC or DC inputs during stress mode based on control signals. The ring oscillator input can also be toggled each stress period to measure the circuit recovery with stress in alternating inverter stages. Stress mode control #2 disconnects the ring oscillator during stress mode to allow for various stress inputs. The table in Fig. 5 lists the control signals and corresponding measurement and stress modes. A 5-bit binary weighted switched capacitor stage is used for the frequency trimming. The desired counter output N is set prior to the stress experiments by scanning in control signals S0-S4. Fig. 6 shows the phase comparator used for detecting the beat frequency. A delayed output of the reference ring oscillator signal is used for the CLK. When CLK is low, the phase comparator is in precharge mode and resets PC_OUT. When the CLK switches to '1', the PC_OUT is determined based on the arrival time of the two inputs signals, ROSC_REF and ROSC_STRESS. Fig. 7 shows the simulation waveforms of the reliability monitor during the measurement mode. The measurement time corresponds to the beat signal period which is 358ns for the 105 stage ring oscillators with an initial counter output of 256. This time is short enough that the amount of unwanted recovery during the measurement can be ignored [3]. Multiple counter outputs are sampled in a single measurement for data post-processing. Stress time versus reliability monitor output and frequency degradation is plotted in Fig. 8. The sensor output changes by 139 for a 0.45% frequency degradation after the first stress period. The die area of the 130nm CMOS test circuit was 0.035mm^2 (Fig. 9).

Acknowledgements

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References

[1] M. Denais, A. Bravaix, V. Huard, et al., "On-the-fly characterization of NBTI in ultra-thin gate oxide PMOSFET's", *IEDM,* pp. 5.2.1-5.2.4, 2004.

[2] V. Reddy, A. Krishnan, A. Marshal, et al., "Impact of negative bias temperature instability on digital circuit reliability", *IRPS,* pp. 248-254, 2002.

[3] S. Rangan, N. Mielke, E. Yeh, "Universal recovery behavior of negative bias temperature instability", *IEDM,* pp. 14.3.1-14.3.4, 2003.

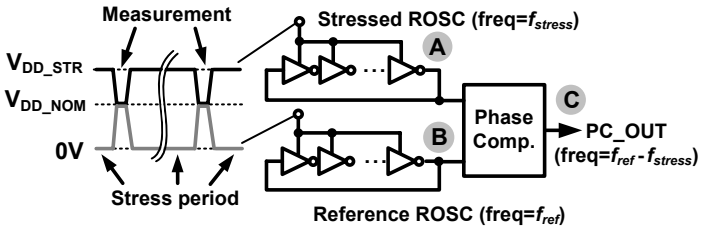


Fig. 1. Proposed beat frequency detection circuit for high resolution reliability monitoring.

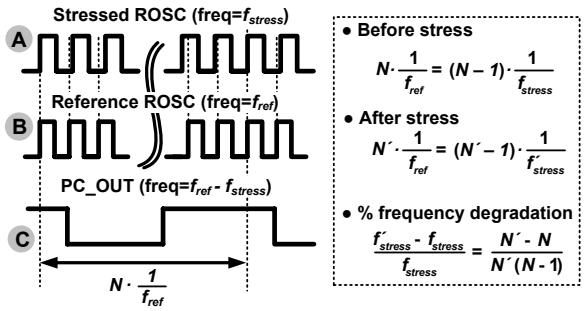


Fig. 2. Principle of proposed beat frequency detection circuit.

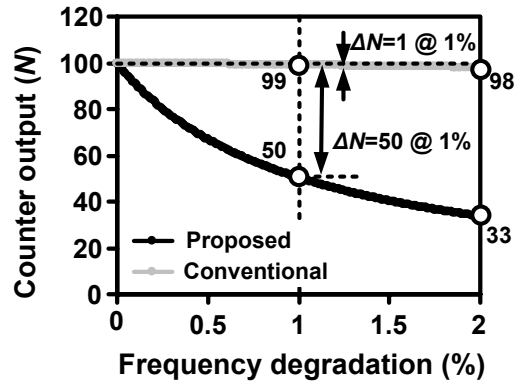


Fig. 3. Sensing resolution comparison. Proposed scheme provides 50X higher sensing resolution for detecting 1% frequency degradation.

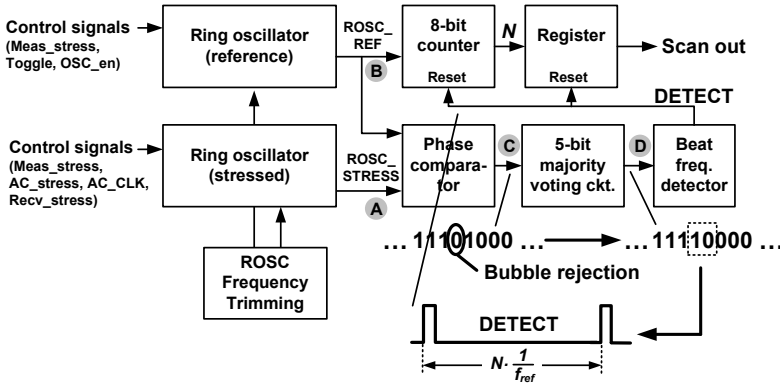
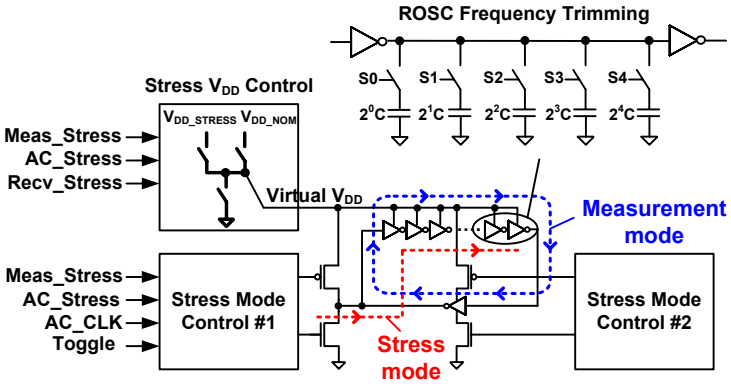


Fig. 4. Reliability monitor test chip architecture.



Mode	Stress condition	Meas_Stress	AC_Stress	Toggle
Measure	N/A	1	D/C	D/C
Stress	DC w/o toggle	0	0	0
	DC w/ toggle	0	0	1
	AC	0	1	D/C

Fig. 5. Ring oscillator circuit and measurement/stress modes.

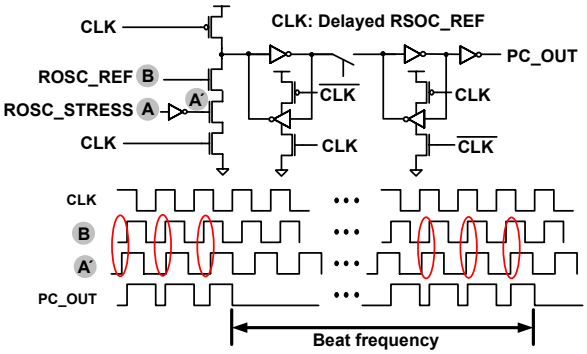


Fig. 6. Phase comparator circuit.

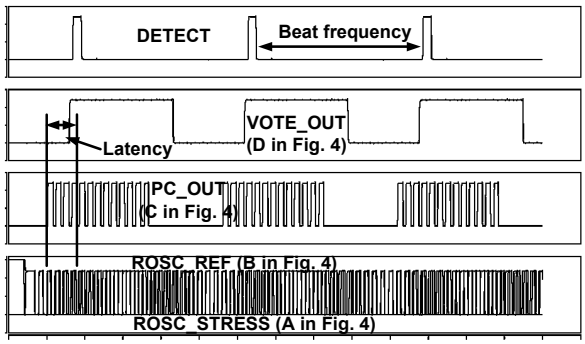


Fig. 7. Simulated waveforms during measurement mode.

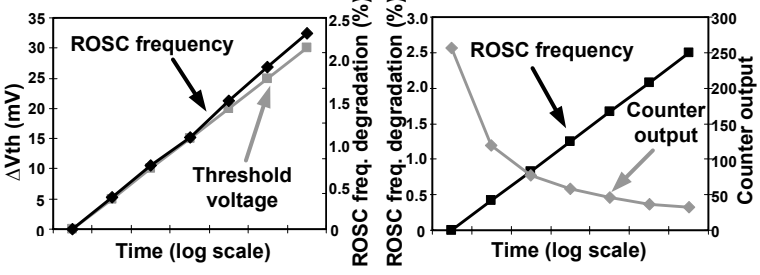


Fig. 8. Stress time versus reliability monitor output.

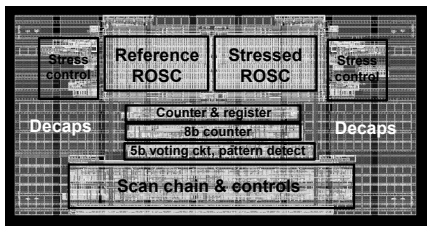


Fig. 9. Layout of 130nm test chip (265x132μm^2).