Silicon Odometer: An On-Chip Reliability Monitor for Measuring Frequency Degradation of Digital Circuits

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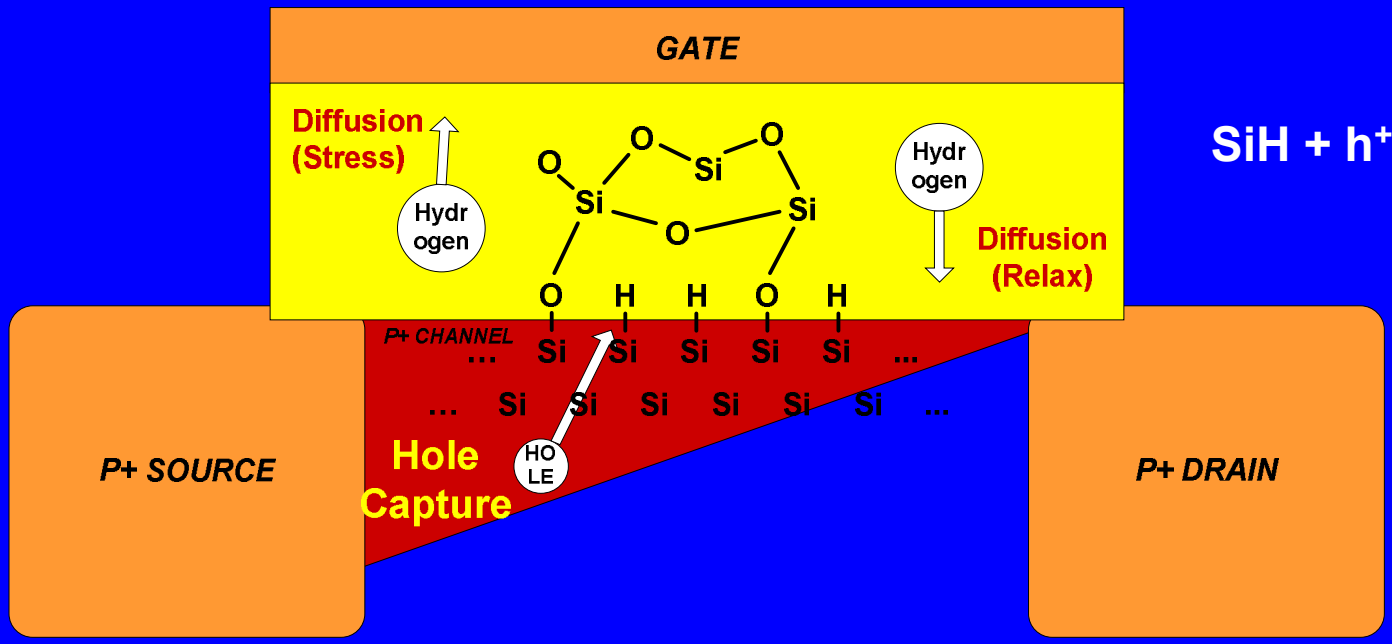
Outline

- NBTI Overview
- Previous NBTI Measurement Method
- Proposed Silicon Odometer Circuit
  - Beat Frequency Detection Scheme
- Test Chip Measurement Results
  - Voltage and Temperature Dependency
  - DC and AC Stress
- Conclusions

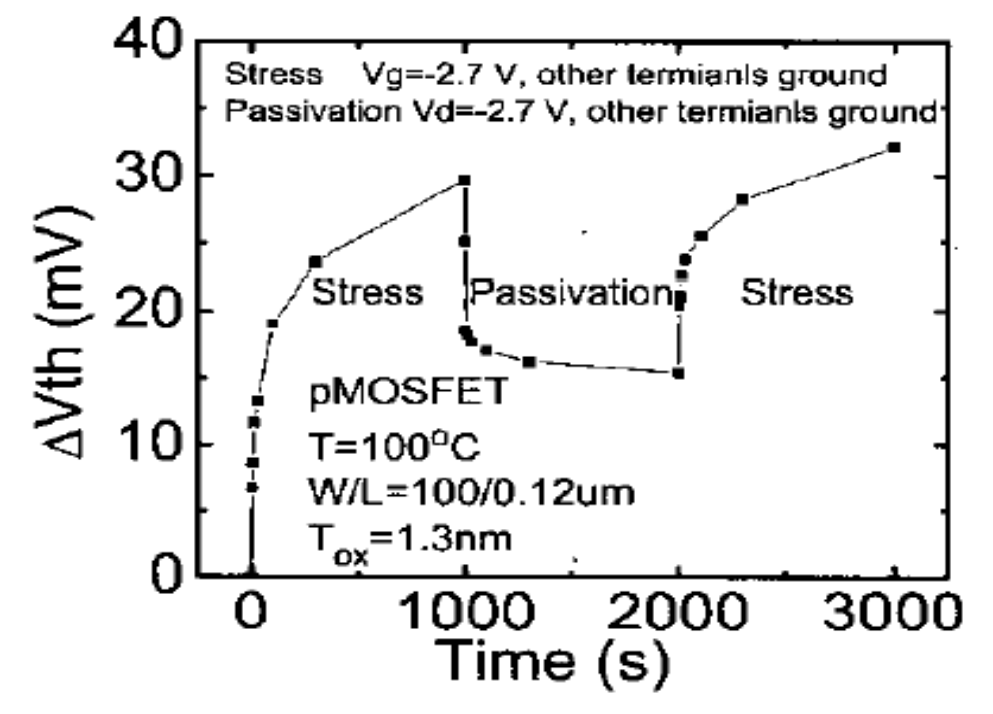
Negative Bias Temperature Instability

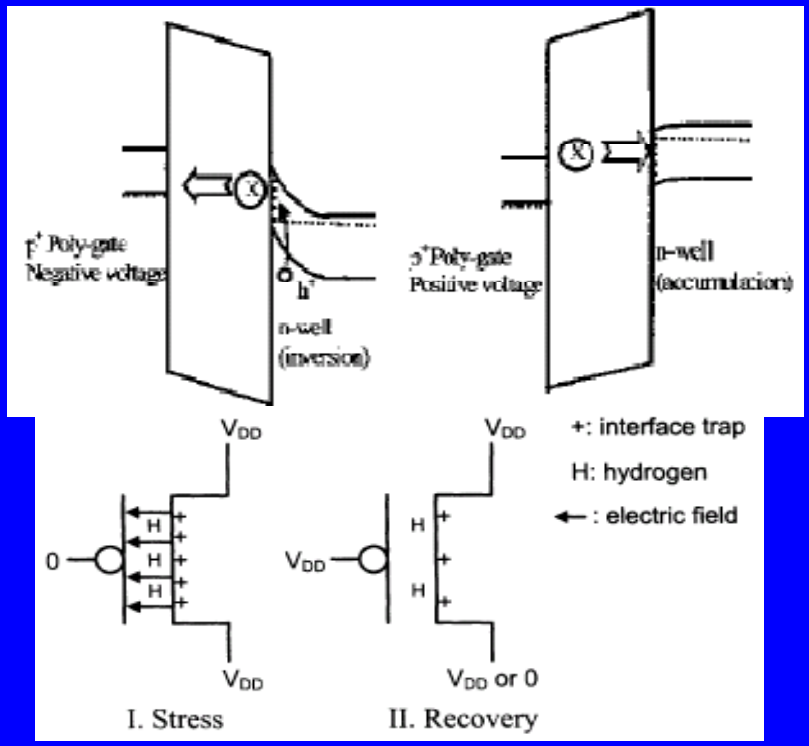


$SiH + h^+ \rightarrow Si^+ + H$

- One of the most critical reliability issues today
- Holes in inversion layer interact with Si-H bonds at interface when device is under stress (V_{gs}= -V_{dd}), → leave interface traps
- NBTI manifests itself as an increase in $|V_{tp}|$

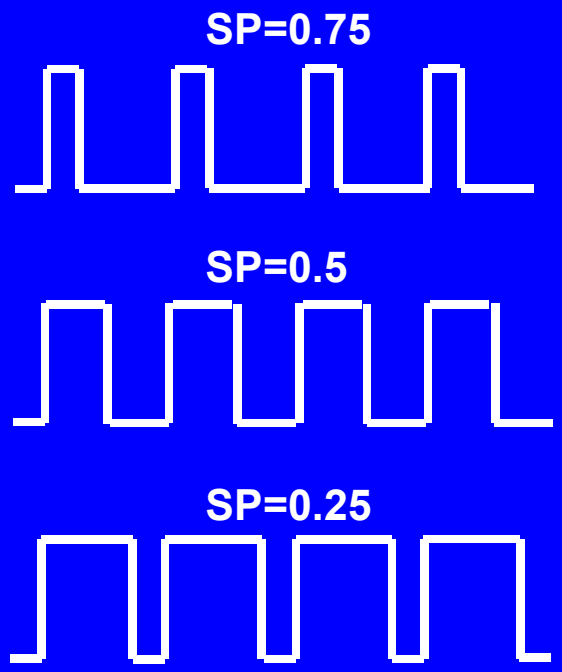
Stress and Recovery

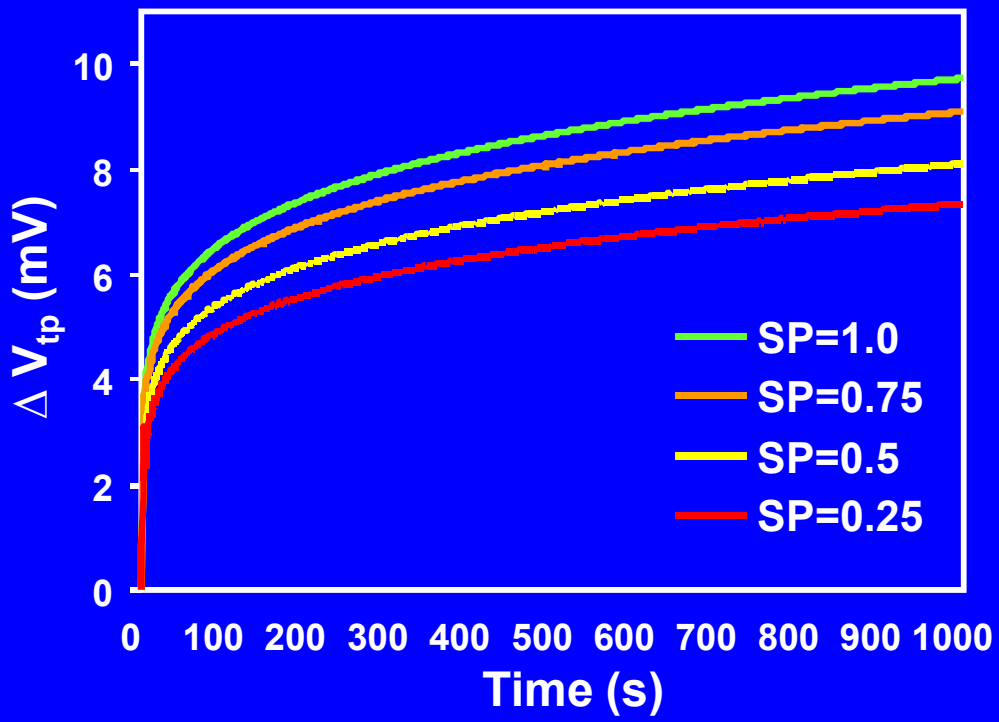




- When a stressed PMOS is turned off
  - Si-H bond breaking stops
  - H diffused back to Si/SiO_2 interface and anneals broken bonds
- AC stress increases lifetime projection
- Increasing field and temperature, reduced gate overdrive reintroduce NBTI concerns in the late 90s

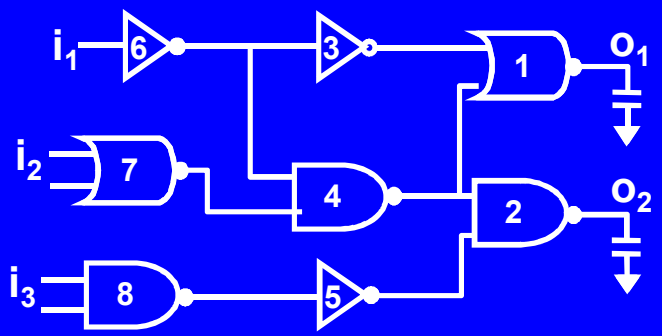
NBTI Signal Probability Dependence

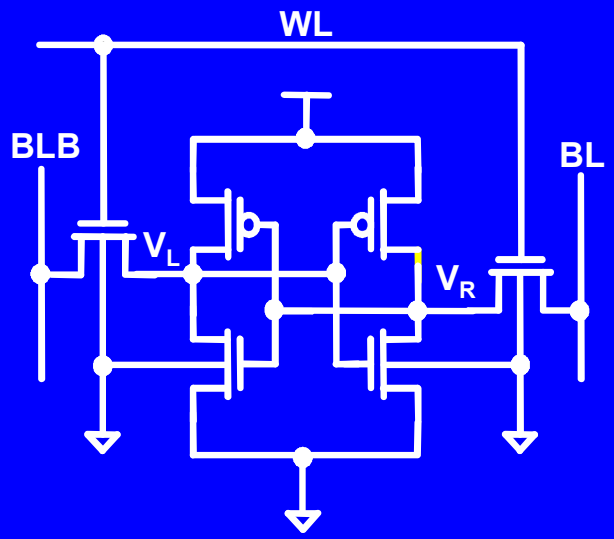




- Device is stressed when input signal is low
- Signal Probability (SP): Probability that the input signal is low
- NBTI effect is SP dependent

NBTI Impact on Digital Circuits





Logic circuits

- F_{MAX} degrades
- Leakage power reduces

Memory circuits

- Read margin worsens
- Write stability improves
- Read delay remains the same

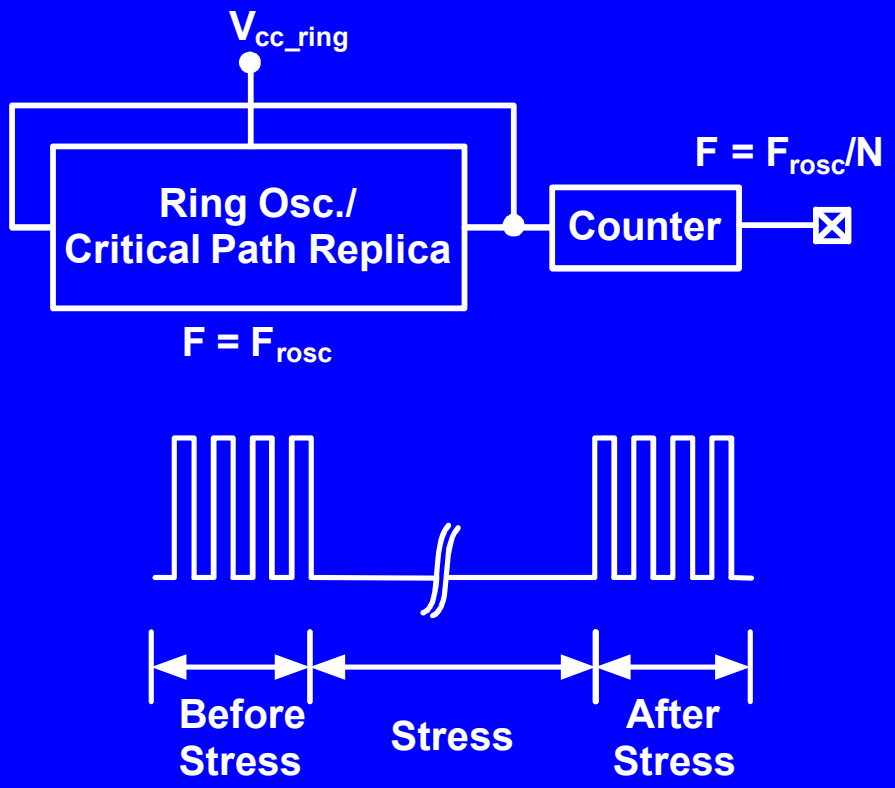
- NBTI affects critical circuit parameters
- Need to design circuits with NBTI-induced shifts comprehended

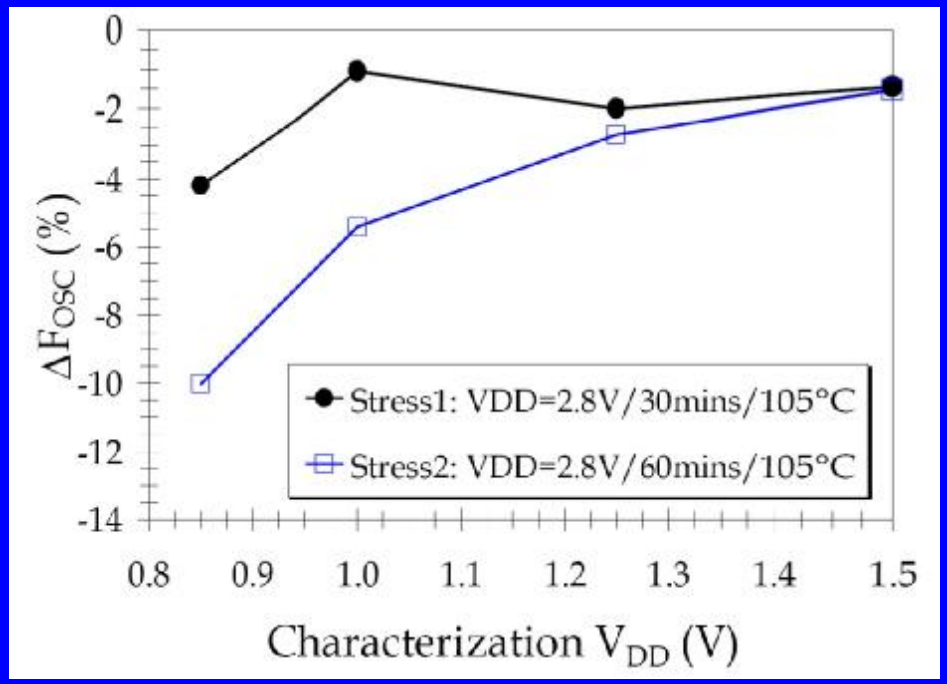
Circuit Techniques to Mitigate the Impact of NBTI Degradation

- Product margin-testing, guard-banding
- Size up devices
  - Negates benefits of scaling, increases power
- Toggle circuit nodes
  - Less degradation under AC stress
- Lower temperature
  - Difficult task now…dense/fast designs are hot
- Progressive V_{tp} and V_{dd} tuning
  - We can slowly increase V_{dd} or forward body bias PMOS as performance degrades with aging (Intel, ISSCC07)

Bottom line: Need to accurately measure the NBTI effect and develop compact models

Previous NBTI Measurement Technique

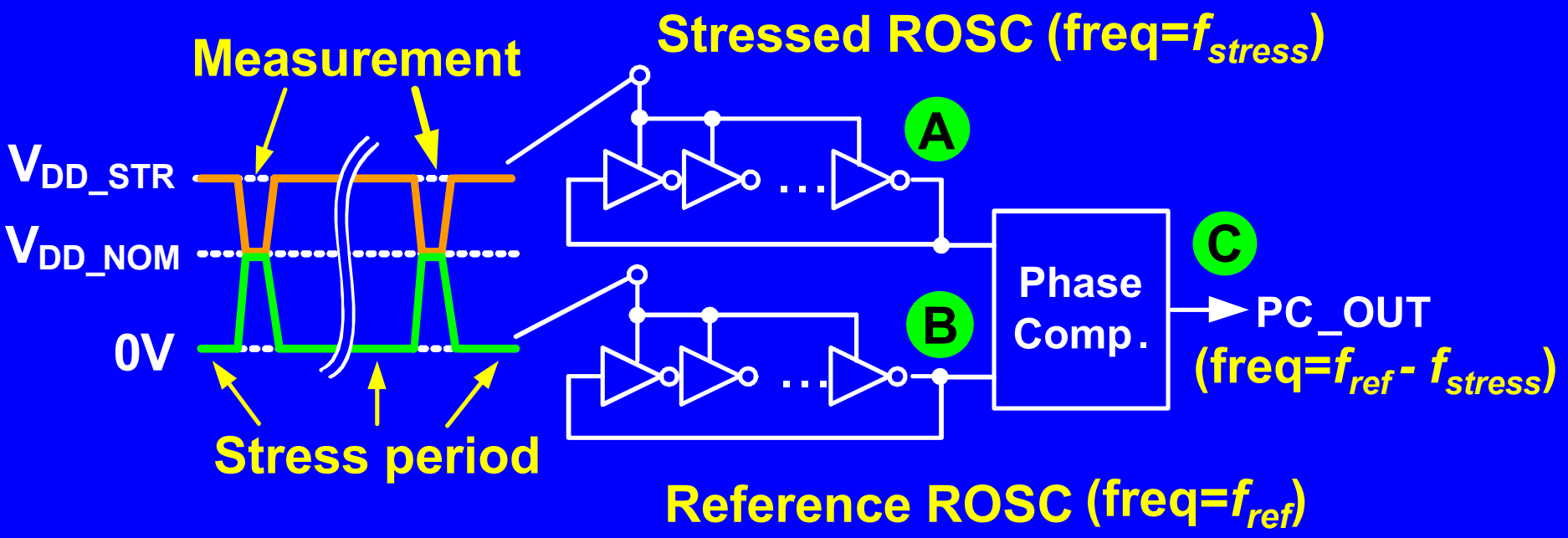




V. Reddy et al., IRPS, 2002

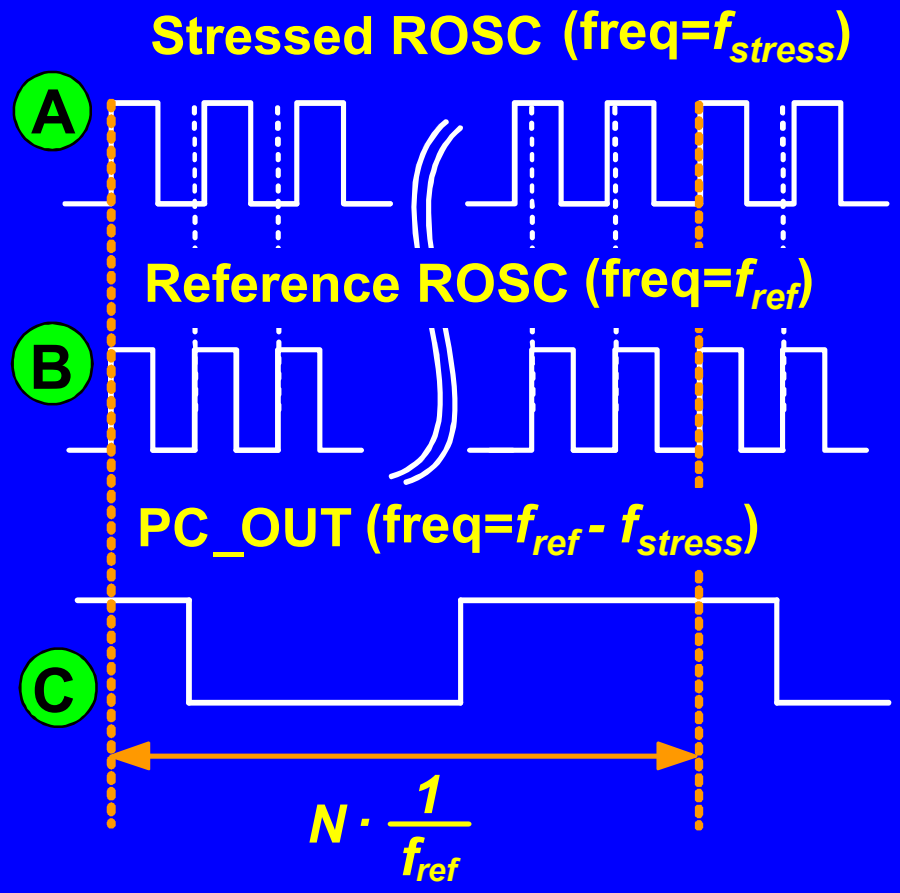
- Measure ring oscillator frequency shift
- Main limitations
  - Low sensing resolution (few % frequency change)
  - Sensitive to environmental variation during measurement
  - Invasive, not suitable for run-time monitoring

Proposed Silicon Odometer Circuit



- Two free running ROSCs for beat frequency detection
- Sample stressed ROSC output using reference ROSC output
- Count PC_OUT to determine frequency degradation
- Insensitive to environmental variation

Principle of Silicon Odometer Circuit



- Before stress

$$N \cdot \frac{1}{f_{ref}} = (N-1) \cdot \frac{1}{f_{stress}}$$

- After stress

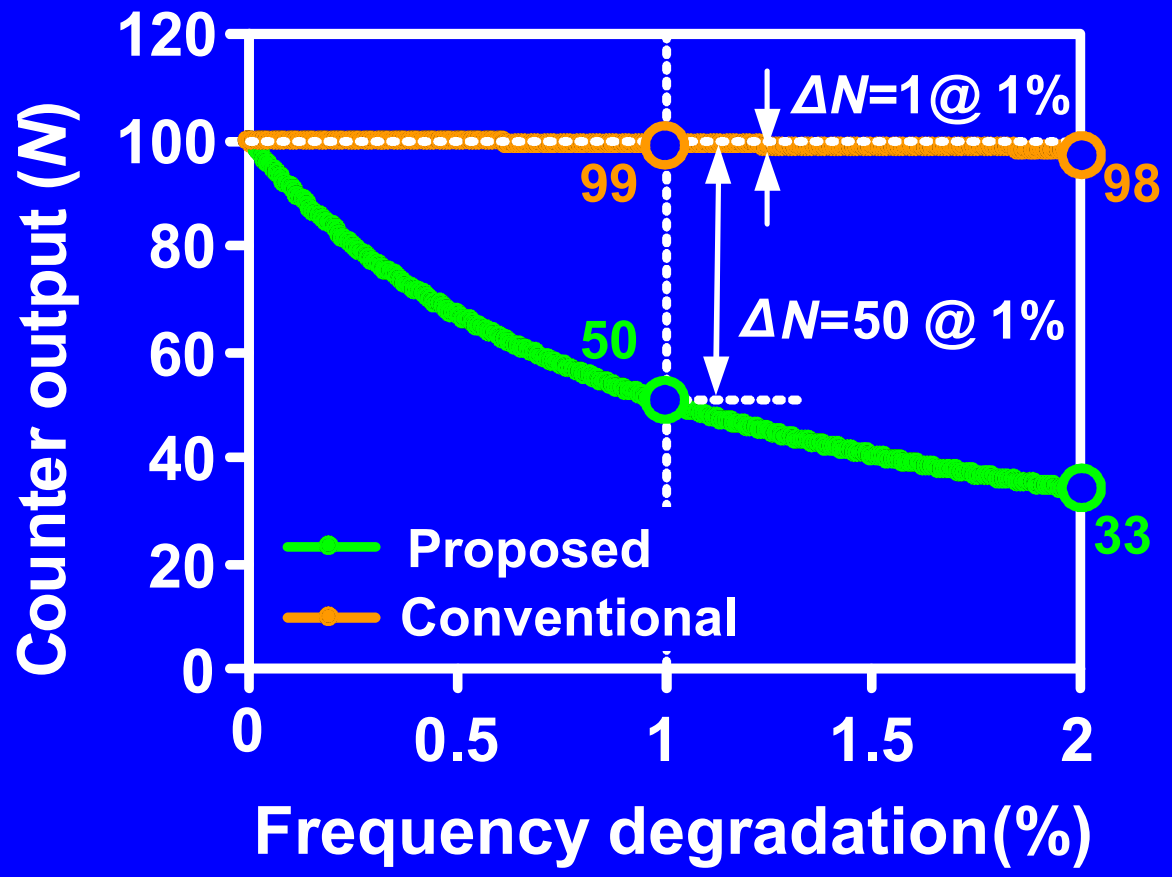
$$N' \cdot \frac{1}{f_{ref}} = (N'-1) \cdot \frac{1}{f'_{stress}}$$

- % frequency degradation

$$\frac{f'_{stress} - f_{stress}}{f_{stress}} = \frac{N' - N}{N'(N-1)}$$

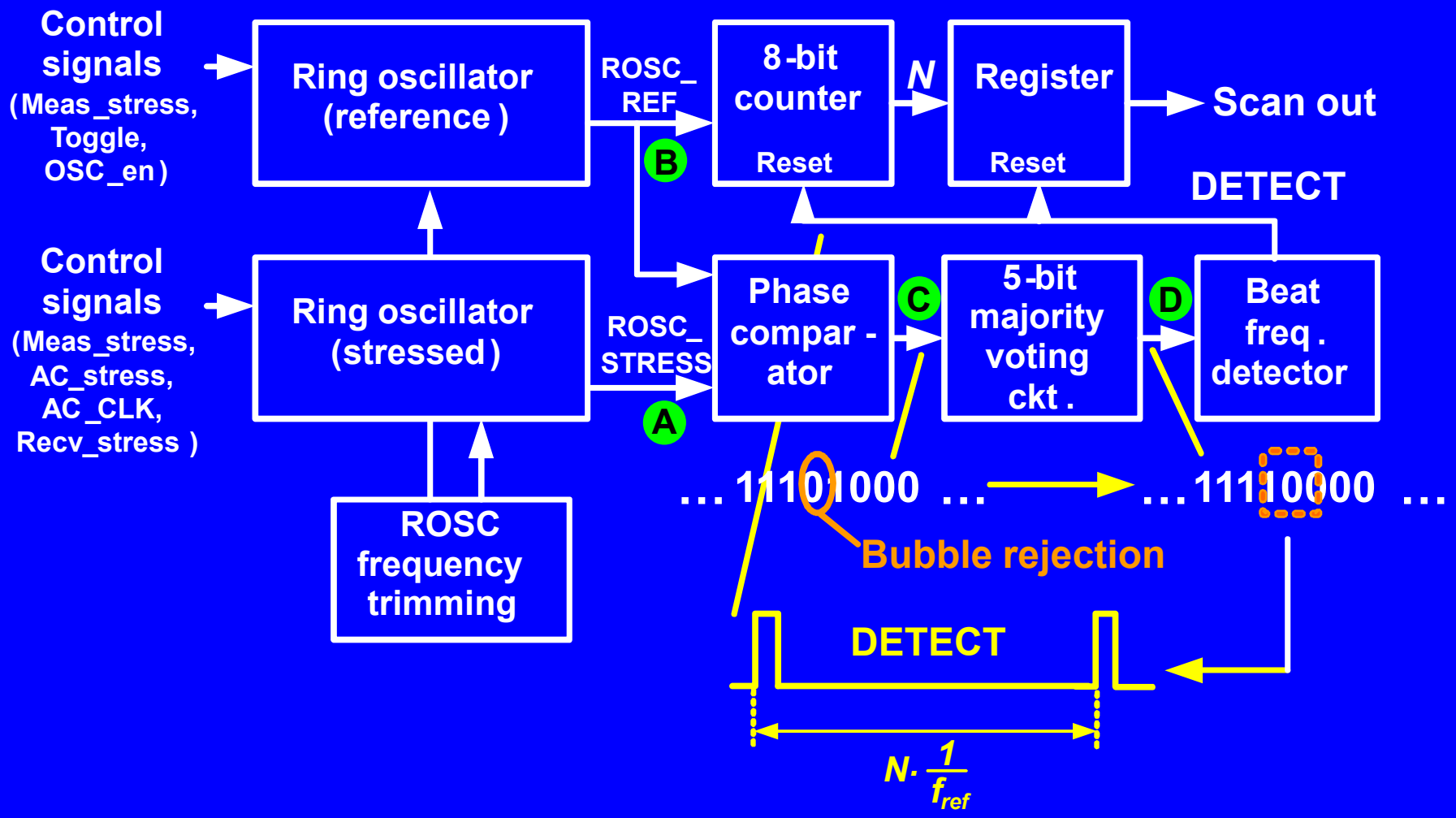
- **Operation example**
  - 1% delay difference before stress → N = 100
  - 2% delay difference after stress → N´ = 50
  - N´ changes by 50 for 1% change in delay → sub-ps resolution degradation measurements

Sensing Resolution Comparison



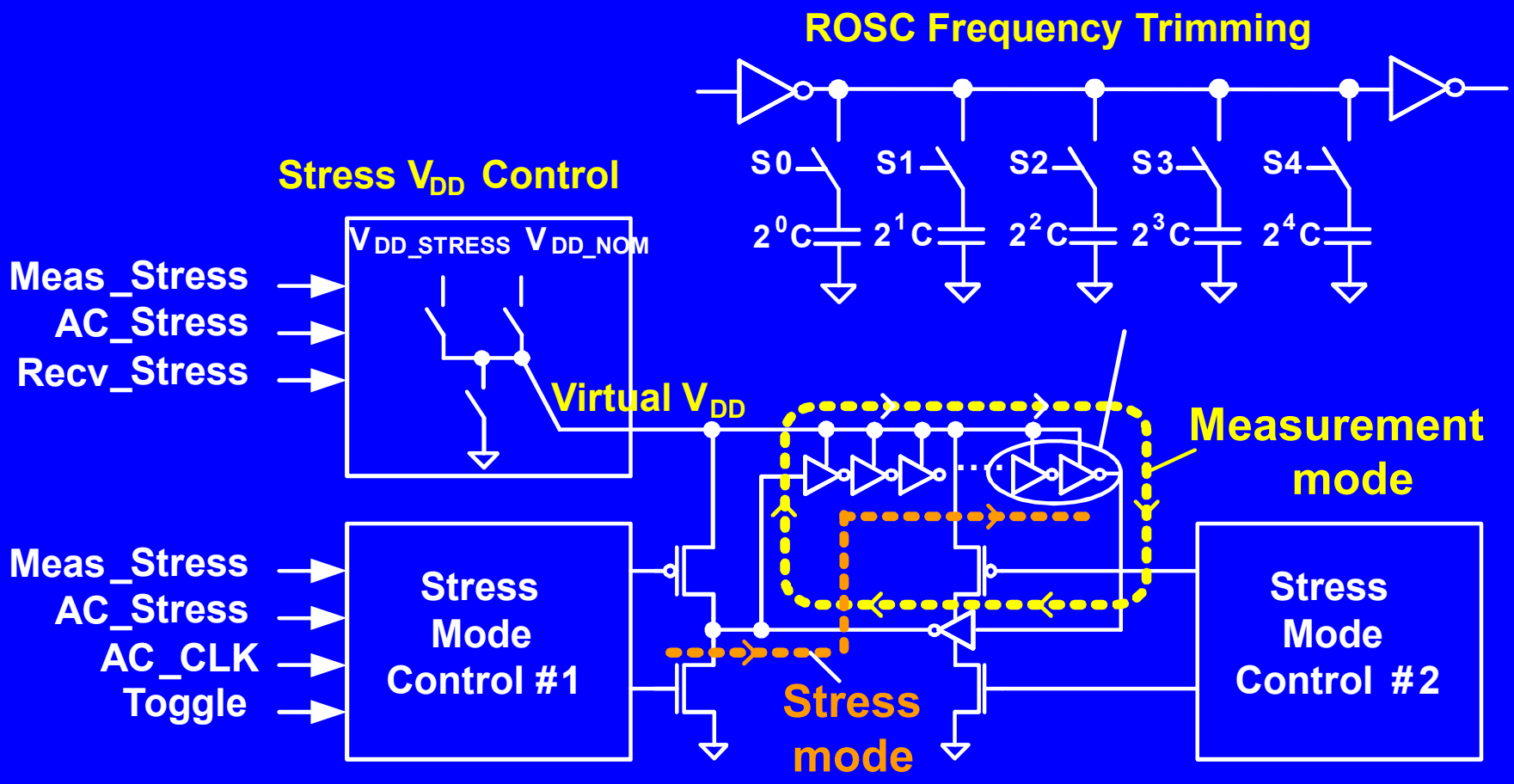
- **High delay sensing resolution**
  - For N=100 and T=4ns, maximum sensing resolution is 0.4ps (0.01%)

Test Chip Architecture



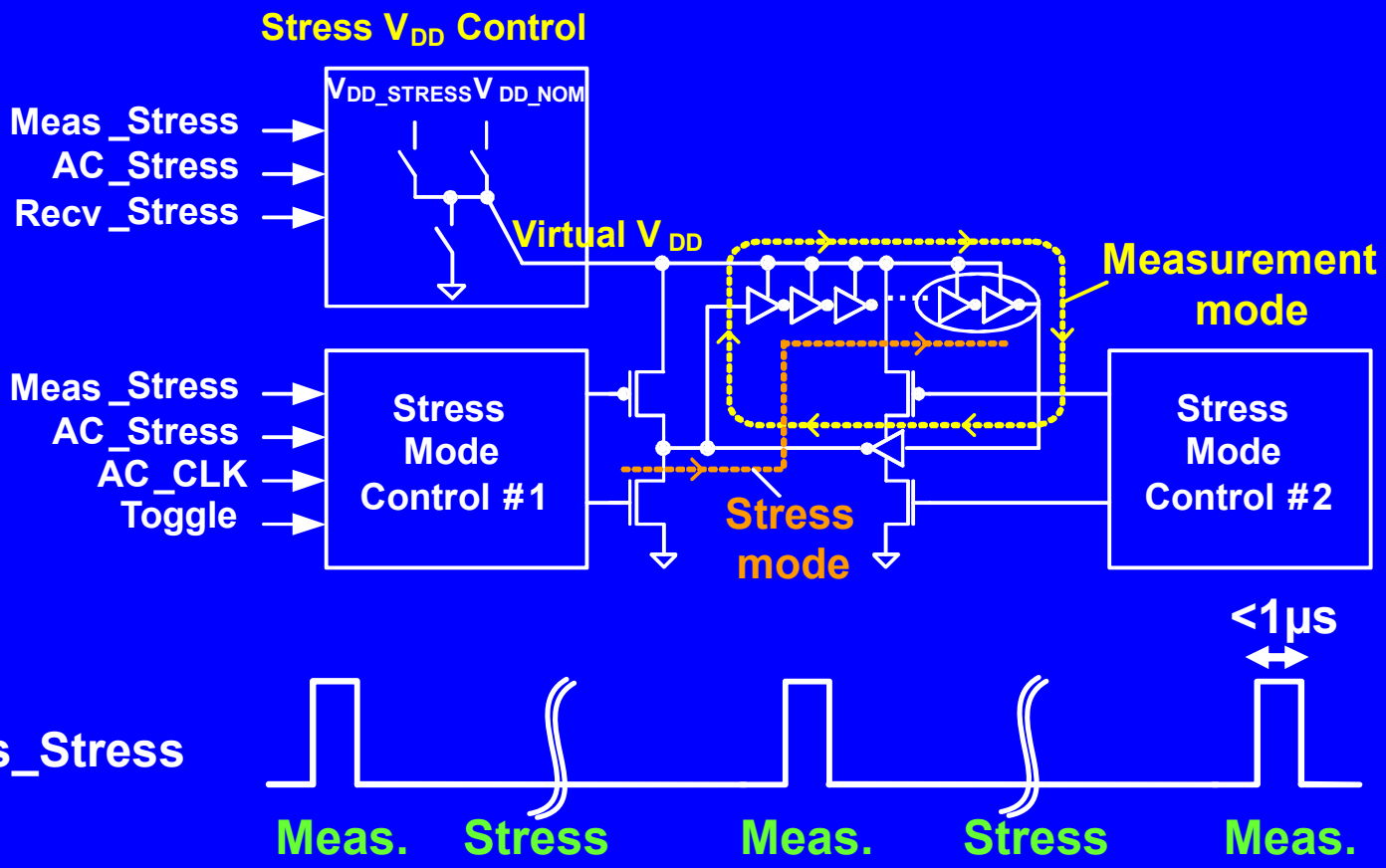
- Frequency trimming capacitors set the initial frequency difference between the stressed and reference ROSC
- 5 bit majority voting circuit for bubble rejection

Ring Oscillator Circuit Design



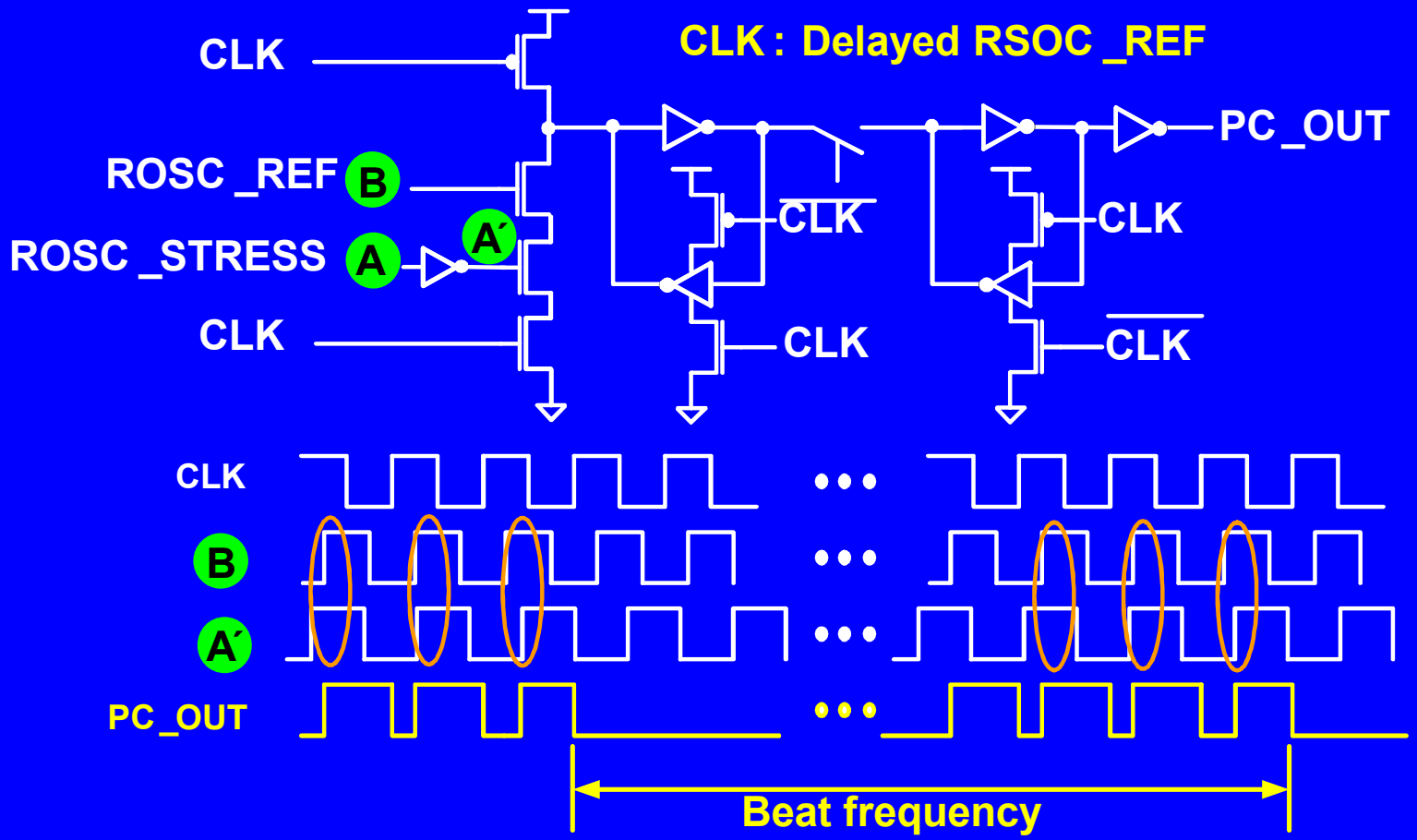
- 4ns ROSC period, frequency trimming capacitors
- Stress mode and measurement mode
- Meas_Stress triggers the measurement

Various Stress/Recovery Modes



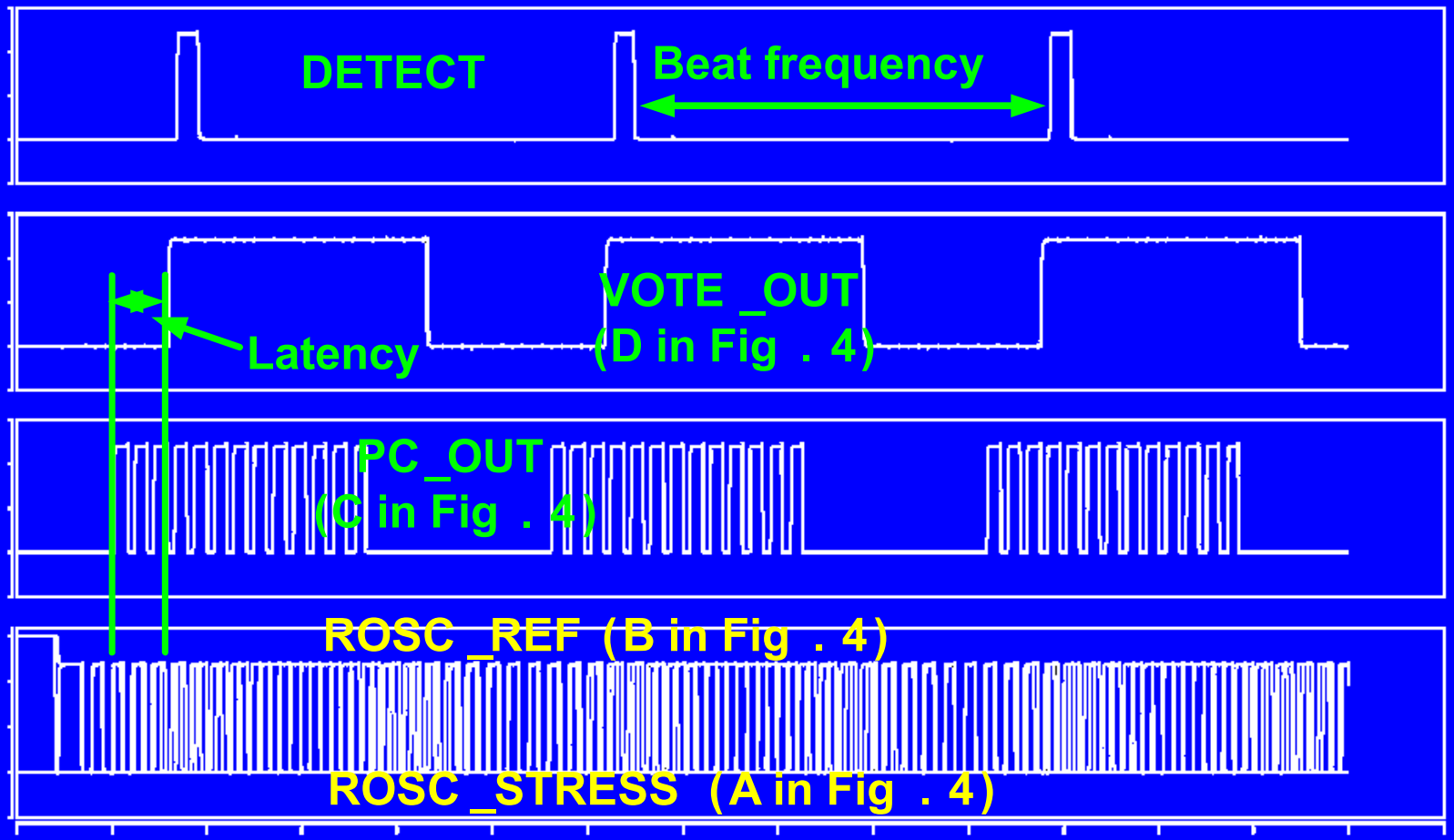
Stress Mode	Meas_Stress	AC_Stress	Toggle
DC_Stress w/ toggle	1	0	1
DC_Stress w/o toggle	1	0	0
AC_Stress	1	1	X
Measurement	0	0	X

Phase Comparator Circuit Design



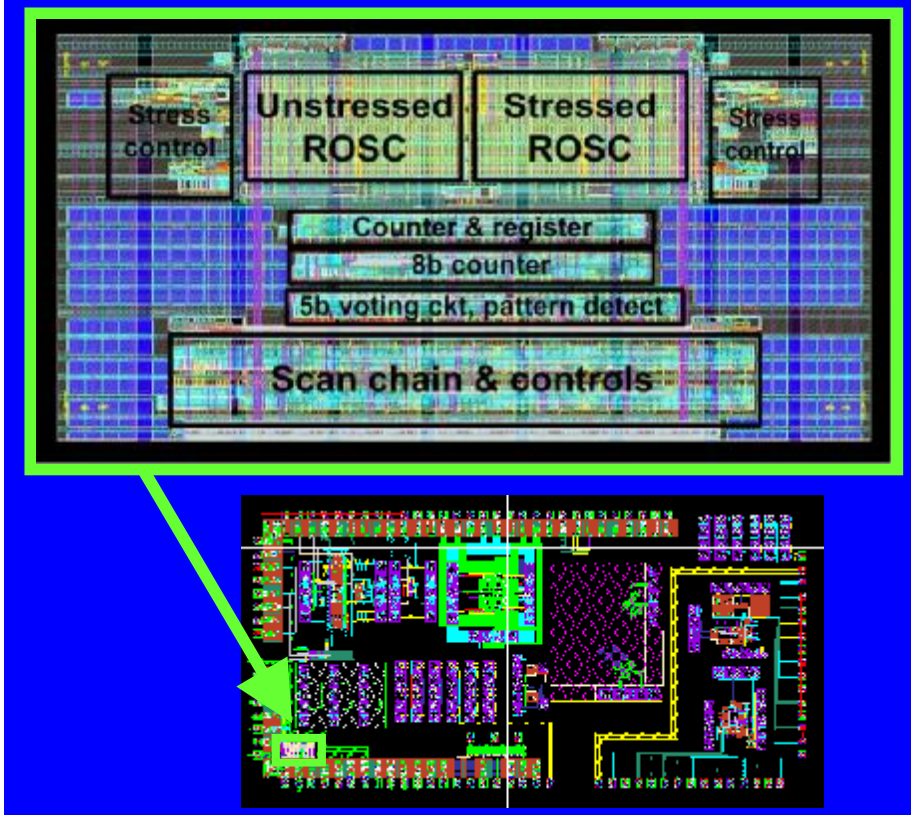
- Delayed ROSC_REF used as reference clock
- Dynamic circuit implementation
- PC_OUT contains the beat frequency

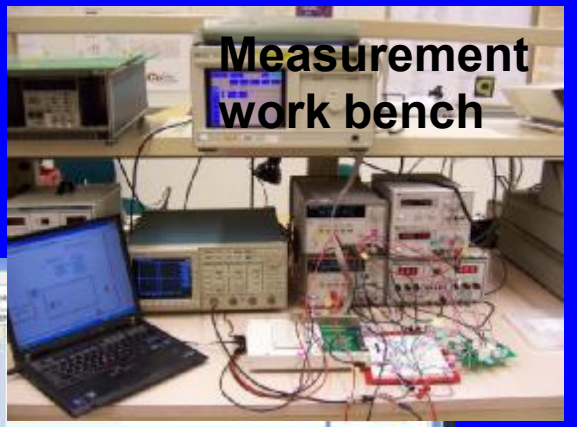
Simulated Waveforms

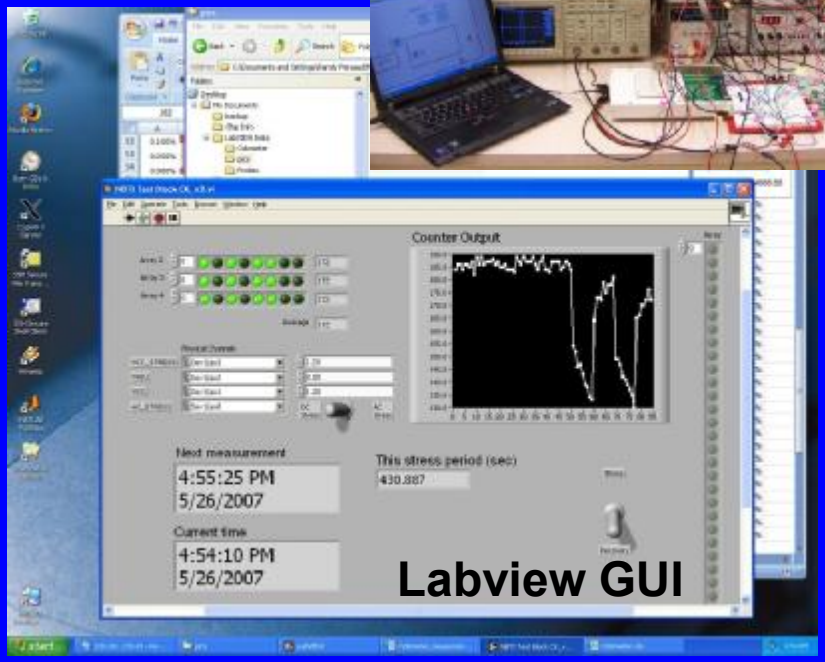


- 3 ROSC cycles of measurement latency
- Static signal from 5b majority voting circuit
- DETECT signal gives beat frequency

Test Chip Implementation



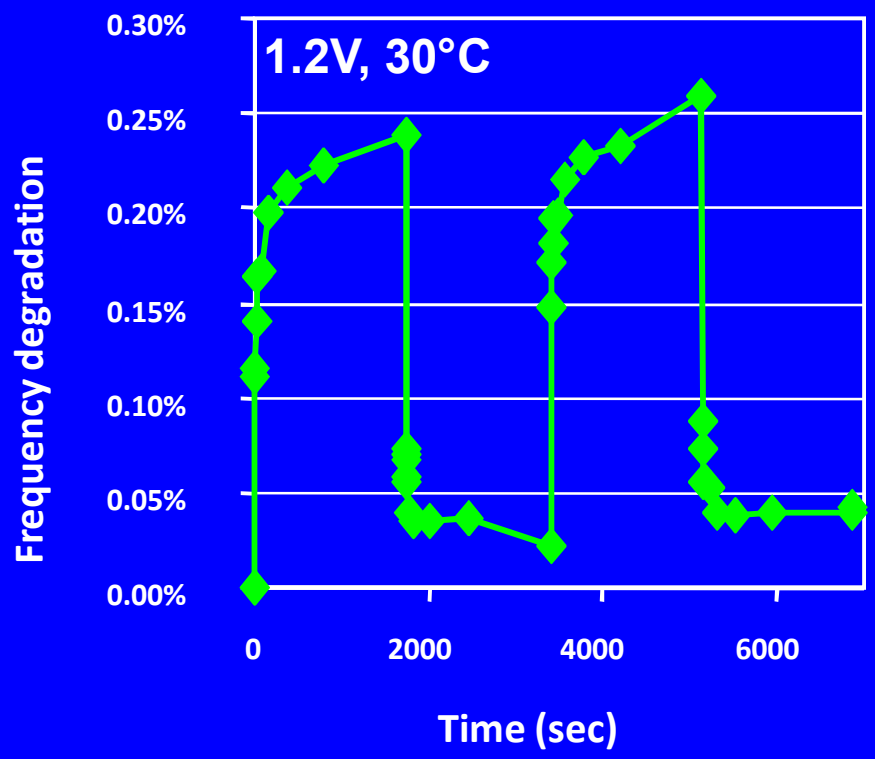




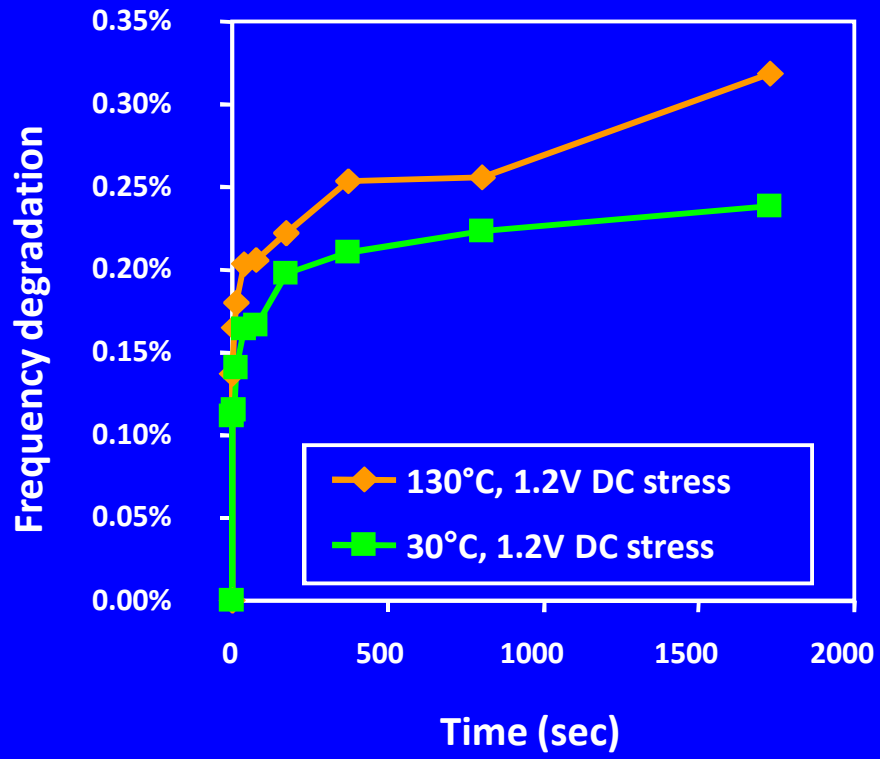
- 0.13μm MM/RF CMOS, 265 x 132 μm^2 layout area
- Stressed and reference ROSCs have identical layout
- Chips were not recycled since once stressed, they will not fully recover

Odometer Measurement Results

Stress and recovery behavior

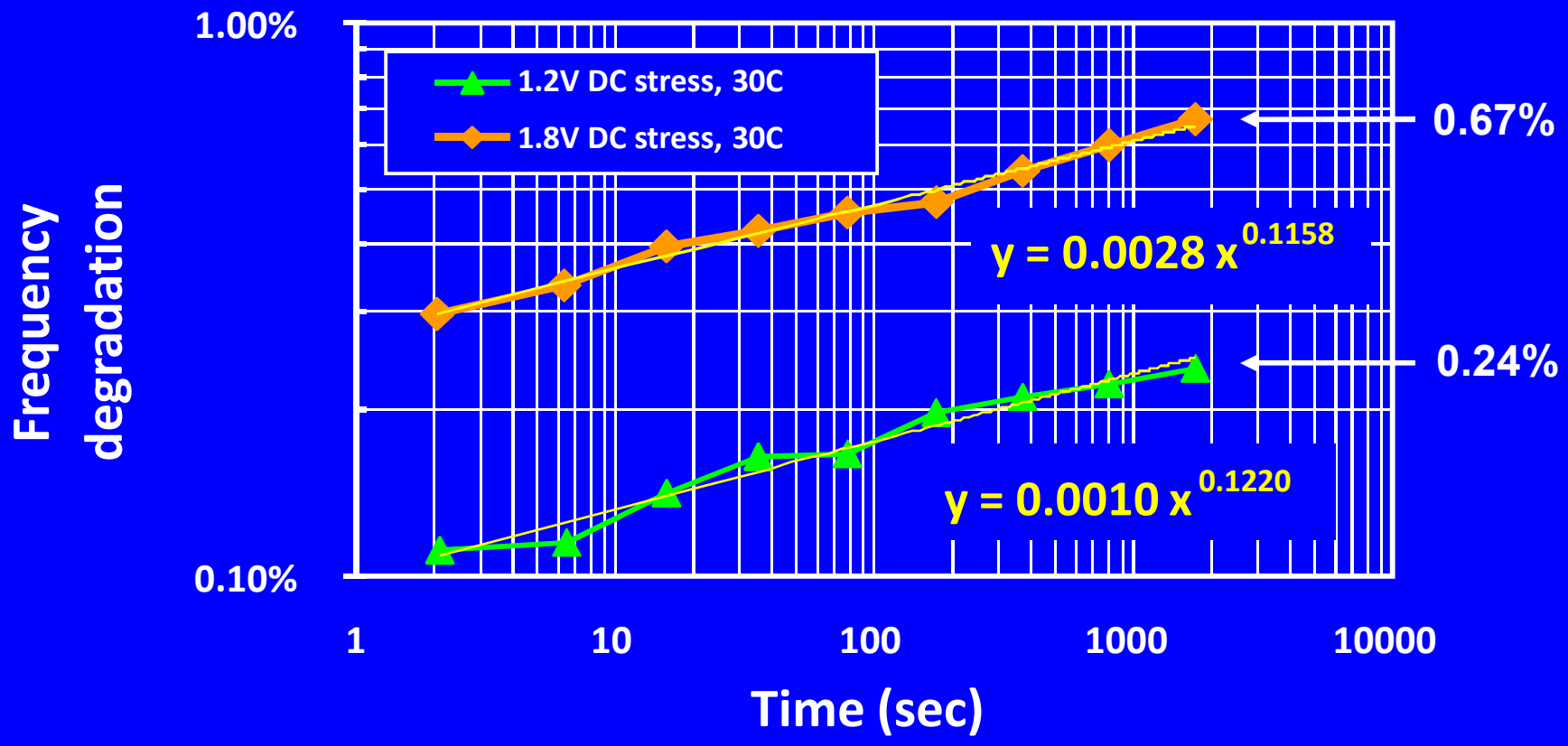


Temperature dependency



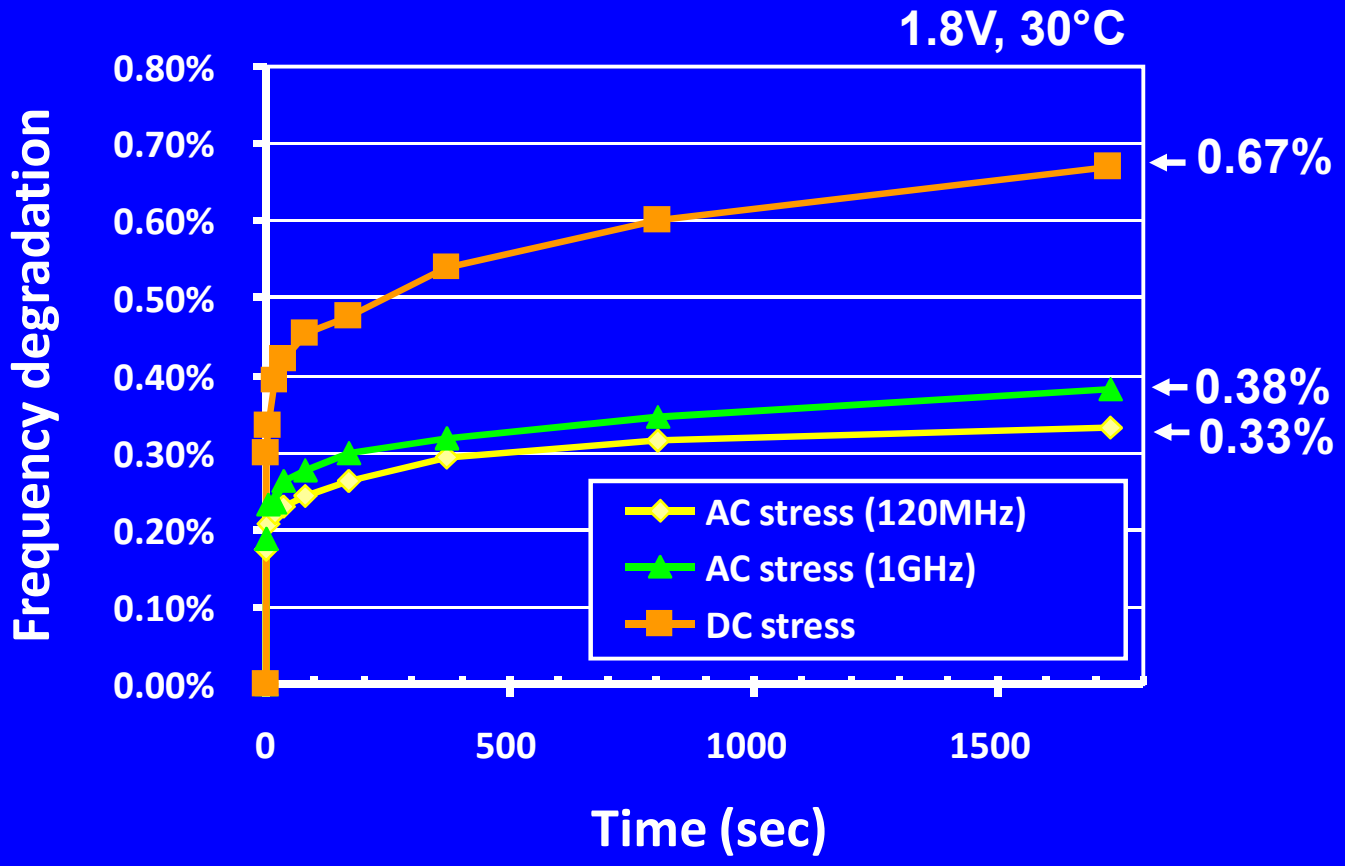
- Resolution high enough (<0.02% or <0.8ps) for non-accelerated stress measurements
- 80% recovery rate due to relatively thick T_{ox}
- Worse degradation at higher temperature

Stress Voltage Dependency



- Degradation exponentially dependent on the electric field
- Delay degradation has same power-law dependency as ΔV_{tp}

DC Stress versus AC Stress



- AC stress results in 43-50% less frequency degradation
- Weak frequency dependency
  - Many baby steps takes you same distance as a few giant steps
- This behavior also confirmed by recursive RD models

Conclusions

- **NBTI is a growing threat to circuit reliability**
- **On-chip NBTI monitor circuits are needed to understand aging impact on circuits**
- ***Silicon odometer* circuit demonstrated**
  - **Fully digital, minimal calibration**
  - **Sub-picosecond sensing resolution**
  - **Sub-microsecond measurement time for minimal annealing**
  - **Differential measurement eliminates common-mode environmental variation impact**

Acknowledgements:

IBM for financial support and UMC for chip fabrication