A Switched Decoupling Capacitor Circuit for On-Chip Supply Resonance Damping

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Abstract

A low power switched decoupling capacitor circuit is proposed to suppress on-chip resonant supply noise. Compared to previous analog techniques, the proposed digital implementation achieves a 9X reduction in quiescent power with improved tolerance to PVT variation and tuning capability for optimal switching threshold. Measurements from a 0.13µm test chip show an 11X boost in effective decap value and a 9.8dB suppression in resonant supply noise by using the proposed circuit.

Introduction

On-chip resonant supply noise caused by package inductance and on-chip capacitance poses a severe threat to system performance because of its large magnitude and long duration. The resonant noise, typically in the 40-200MHz band, can be excited by a microprocessor loop command or a large current surge during an abrupt start-up or termination [1, 2]. Conventional decoupling capacitors (decaps) are inefficient to suppress resonance because of the large die area and gate leakage consumption. This paper presents a low power digitally controlled switched decap circuit to suppress the resonant noise. Unlike prior work that employs differential amplifiers to sense supply noise [3], the proposed scheme uses digital circuits for noise detection to reduce power consumption. A 9X reduction in quiescent power is achieved with improved tolerance to process-voltage-temperature (PVT) variations and added tuning capability for switching threshold. The proposed circuit can be embedded into digital IC's without requiring any extra power supplies or bias voltages.

Proposed Switched Decap Circuit

The principle of the proposed switched decap circuit is shown in Fig. 1. In the absence of resonant noise, the two capacitors are connected in parallel storing the maximum amount of charge and serving as conventional decaps. When a supply droop greater than the switching threshold V_{SW} is detected, the decaps switch to a series connection with charge dumped into the supply network to compensate the supply droop. Vice versa, during a supply overshoot, charge is removed from the supply network by switching the capacitors back to parallel. Because the delivered charge of a switched decap ($=0.5C\cdot Vdd + C\Delta Vdd/2$) is much larger than that of a conventional decap ($=2C\cdot\Delta Vdd$), a decap boost is achieved. Fig. 1 shows the decap boost factor as a function of V_{SW} assuming an ideal control scheme where the suppressed noise magnitude ΔVdd is equal to V_{SW}. A V_{SW} between 25mV to 60mV leads to a decap boost between 5X to 13X. An optimal V_{SW} can be chosen to attain a maximum decap boost while minimizing the unnecessary decap switching caused by minor supply fluctuations. In real implementation, ΔVdd is also determined by the delay of control circuits and deployed decap values. Fig. 2 shows the schematic of the switched decap circuit with a digital resonant detection scheme. The noise detection is realized by comparing the delay of a constant delay line (CDL) and a variable delay line (VDL). The supply of the CDL (Vdd') is low-pass filtered so that the delay is insensitive to supply droop within the range of regulation frequency (>10MHz). The supply of VDL is directly connected to the noisy Vdd so that its delay varies with supply fluctuations. Starved inverters are used for each delay stage to enhance the delay sensitivity to supply noise. Layouts of CDL and VDL are matched to minimize the impact of within-die variation. In the absence of supply noise, the CDL runs slower than the VDL due to the DC supply drop ($V_{SW}=I_{DC}\cdot R$) through the RC filter. When supply droop is equal to V_{SW}, both circuits run at the same speed and a switch signal SW is issued from the phase comparator to trigger the switching of the decaps. When supply voltage rises above $Vdd-V_{SW}$, the switched decaps return to normal configuration to restore charge. The simulated resonant damping performance in Fig. 3 proves that the proposed switched decap performs more than 8X better than a conventional decap. Under process variation, the change of R value ($\propto 1/(Vdd-V_{Tp}-V_{Tn})$) tracks the change of I_{DC} ($\propto Vdd-V_{Tp}-V_{Tn}$) leading to a process insensitive V_{SW} ($=I_{DC}\cdot R$). Simulation result in Fig. 4 confirms a V_{SW} variation of less than 8mV across different process corners (±25mV of V_T) and temperatures (25-110ºC). To enable a fine tuning of V_{SW}, the R value can also be programmed by turning on different number of MOS devices in the RC filter circuits. The proposed circuit is designed with a resonant regulation range of 10MHz-300MHz.

Resonant Noise Measurements

A test chip has been fabricated in a 1.2V, 0.13µm CMOS process. Fig. 5 shows the test chip organization. To generate a resonant supply noise, four 16-bit multipliers with operating frequencies up to 1.0GHz were synthesized and implemented using standard cell libraries. A clock pattern controller is used to create a gated clock which can produce noise components at lower frequencies. A 16-bit clock code is scanned into the controller to set the gated clock pattern. A '1' passes a clock pulse while a '0' masks the clock pulse. As the examples shown in Fig. 6, a '0101010101010101' produces a sub-harmonic noise at 1/2 of the original clock frequency while a '0000111100001111' produces sub-harmonic at 1/8 of the clock frequency. For testing purposes, we also implemented a simple noise injection circuit that generates supply noise at a given clock frequency. Different values of switched decaps (100pF, 200pF, 300pF) can be selectively activated for performance comparison. A noise sensor with a 4dB gain and 900MHz bandwidth is implemented to measure on-chip differential supply noise Vdd-Gnd. Fig. 7 shows the measured noise magnitude in the frequency domain for different switched decap values. The results show a 2.2-9.8dB reduction of resonant supply noise near the 40MHz resonance using 100-300pF switched decaps. Table 1 summarizes the measured performance of proposed switched decap circuits compared with the equivalent conventional passive decaps and damping resistance. An 11X decap boost with 9.8dB resonant noise suppression has been achieved using the proposed circuit. To achieve the same damping effect, previous technique requires a 0.1Ω to 1Ω damping resistance in the supply network leading to an excessive IR droop [1]. Fig. 8 shows the measured noise waveforms using a 16-bit multiplier clocked at 625MHz. For a clock pattern of '1111111111111111', the resonance was not excited due to the high clock frequency. A clock pattern of '0000000011111111', however, excited the resonance at around 40MHz (≈625MHz/16). With the switched decaps activated, the resonance has been significantly damped. Fig. 9 shows the measured resonant noise magnitude for different V_{SW}'s by varying the R value in the RC filter circuit. As we increase the decap value or reduce V_{SW}, the suppression performance is consistently improved. Fig. 10 shows the die photo and chip specifications. Owing to the digital implementation, a quiescent power consumption of only 0.54mA was consumed leading to a 9X power saving compared to previous work [3]. The proposed circuit including the load decaps is only 11% of the equivalent passive decap implementation leading to an 89% area saving.

Acknowledgements

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[2] E. Hailu, et al., *ISSCC Dig. Tech. Papers*, pp. 548-549, Feb. 2006.

[3] M. Ang, et al., *ISSCC Dig. Tech. Papers*, pp. 438-439, Feb. 2000.

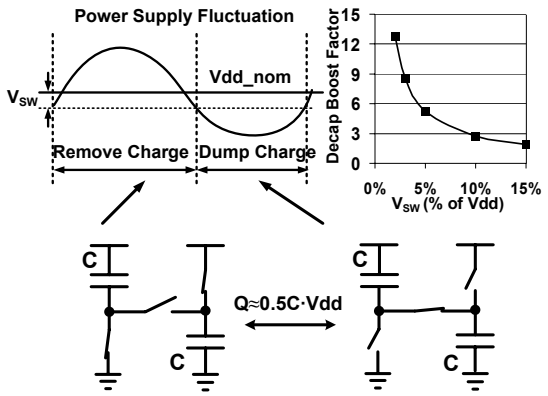

Fig. 1. Principle of resonant noise suppression using switched decaps.

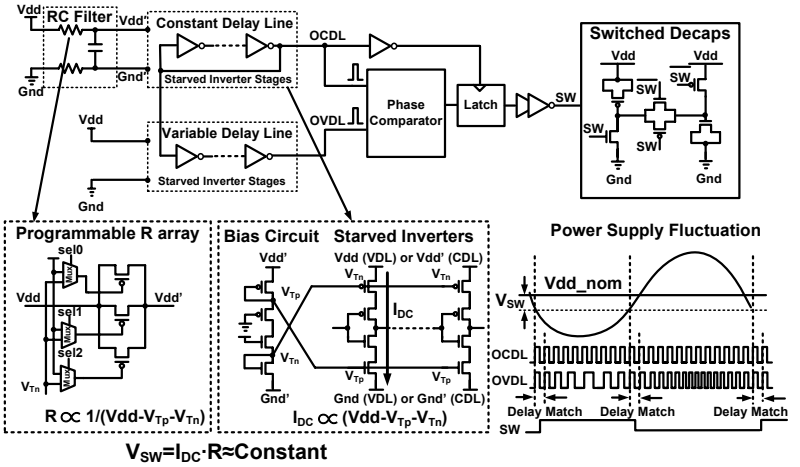

Fig. 2. Proposed switched decap circuit with digitally-controlled resonant detection.

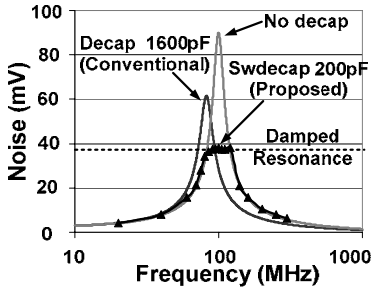

Fig. 3. Simulated decap performance.

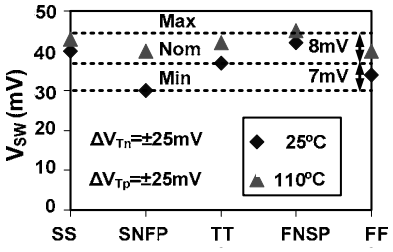

Fig. 4. Simulated V_{SW} change due to process and temperature variations.

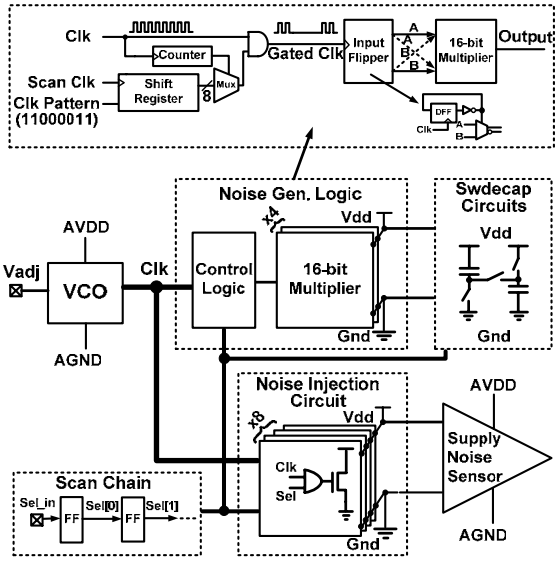

Fig. 5. 0.13µm test chip organization.

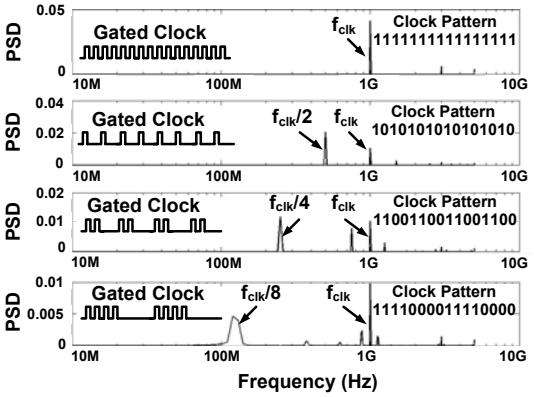

Fig. 6. Simulated power spectrum density from different clock patterns.

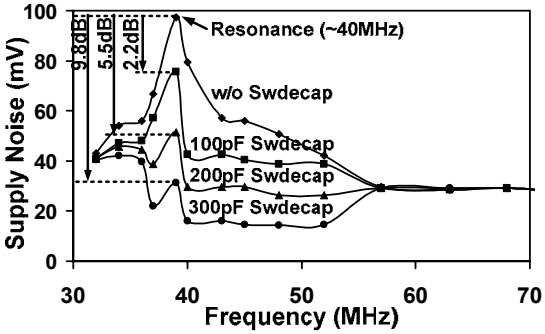

Fig. 7. Measured supply noise in frequency domain near resonant frequency (resonant frequency is shifted compared to Fig. 3 due to larger package inductance).

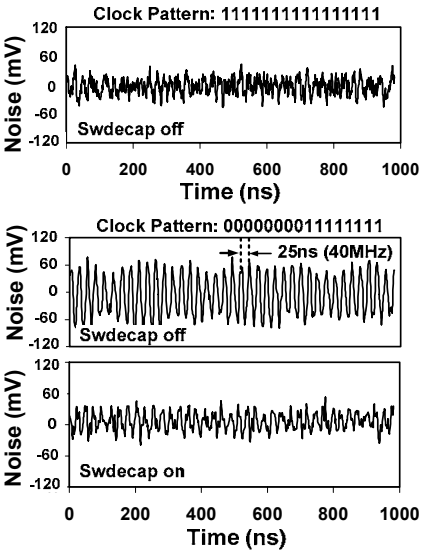

Fig. 8. Measured supply noise waveforms.

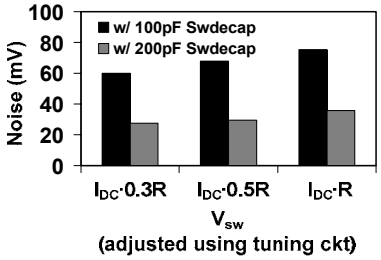

Fig. 9. Measured resonant supply noise for different switching thresholds.

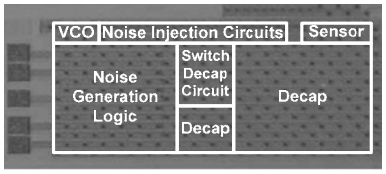

Fig. 10. Test chip die photograph.

Table 1. Summary of measured decoupling effects.

Swdecap Value	Resonant Suppression	Equiv. Passive Decap	Decap Boost	Equiv. Damp. Resistance
100pF	2.2dB	500pF	5X	0.1Ω
200pF	5.5dB	1500pF	7.5X	0.4Ω
300pF	9.8dB	3500pF	11X	1Ω

Technology	0.13µm CMOS
Quiescent Current	0.54mA
Regulation Freq.	10MHz-300MHz
Regulator Area (w/o decap)	100µmx70µm
Regulator Area (w/ 300pF decap)	190µmx220µm
Total Die Area	0.9mmx1.8mm