A 700MHz 2T1C Embedded DRAM Macro in a Generic Logic Process with No Boosted Supplies

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Outline

• Motivation
• Proposed Fully Logic-compatible EDRAM
  – 2T1C Gain Cell with No Boosted Supplies
• Enhancement of EDRAM Retention Time
  – Single-ended 7T SRAM Repair Scheme
  – Storage Monitor for PVT-aware Refresh Control
• 65nm EDRAM Chip Measurements
• Summary
## Embedded Memory Options

<table>
<thead>
<tr>
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<tbody>
<tr>
<td><strong>Cell Schematic</strong></td>
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<td></td>
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<tr>
<td><strong>Process</strong></td>
<td>Logic-compatible</td>
<td>Logic compatible +2 (FEOL)+3 (Cap)</td>
<td>Logic compatible (+2 FEOL)</td>
</tr>
<tr>
<td>Boosted supplies</td>
<td>No required</td>
<td>Required (High &amp; Low)</td>
<td>Required (High &amp; Low)</td>
</tr>
<tr>
<td>Cell size (ratio)</td>
<td>135F² (1X)</td>
<td>30F² (0.22X)</td>
<td>65F² (0.48X) [4]</td>
</tr>
<tr>
<td>Data storage</td>
<td>Latch (Static)</td>
<td>Capacitor (20fF)</td>
<td>MOS gate (&lt;1fF)</td>
</tr>
<tr>
<td>Cell access</td>
<td>(+) Differential read (-) Ratioed operation</td>
<td>(-) Destructive read (-) Refresh</td>
<td>(+) Decoupled read and write, (-) Refresh</td>
</tr>
<tr>
<td>Random cycle</td>
<td>1GHz</td>
<td>500MHz</td>
<td>667MHz</td>
</tr>
<tr>
<td>Static power</td>
<td>1X</td>
<td>0.2X</td>
<td>0.32X @500MHz</td>
</tr>
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</table>


- **Gain cell considered as a strong contender for future embedded memories**
Boosted Supplies in EDRAM

“Asymmetric 2T gain cell”, K. Chun et al., VLSI Symp. 2010

- DRAMs require boosted high and low voltages
  → Special thick $T_{OX}$ devices needed for reliability
- Focus of this work: Eliminating boosted supplies for a fully logic-compatible (single $T_{OX}$) design
Gain Cell with No Boosted Supplies

**Circuit diagram**

<table>
<thead>
<tr>
<th>RWL</th>
<th>RBL</th>
<th>WBL</th>
<th>WWL (this work)</th>
<th>WWL (conv.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hold</td>
<td>VDD</td>
<td>VDD</td>
<td>0V</td>
<td>VDD</td>
</tr>
<tr>
<td>Read 1/0</td>
<td>~0V</td>
<td>VDD-0.2V/VDD</td>
<td>0V</td>
<td>VDD+Δ</td>
</tr>
<tr>
<td>Write 1/0</td>
<td>VDD</td>
<td>VDD</td>
<td>VDD-0.2V/0V</td>
<td>VDD+Δ</td>
</tr>
</tbody>
</table>

Signal levels in each mode

- Δ > 0.4V

- Asymmetric 2T gain cell + Coupling device (PC)

**Diagrams:**

- (ACT~M1)
  - PW
  - Storage
  - PC
  - PS

- (M2~M5)
  - WBL
  - RWLB
  - RWL
  - RBL
  - RSEL
  - PCOU

**Table:**

<table>
<thead>
<tr>
<th>Bit-cell size (μm²)</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>6T</td>
<td>0.575x2.05=1.179</td>
</tr>
<tr>
<td>2T</td>
<td>0.48x0.995=0.478</td>
</tr>
<tr>
<td>2T1C</td>
<td>0.50x1.37=0.685</td>
</tr>
<tr>
<td>7T</td>
<td>1.3x1.37=1.781</td>
</tr>
</tbody>
</table>

*65nm LP CMOS design rule
Retention with No Boosted Supplies

**Conventional 2T**

- 65nm LP, 1.1V, 85°C
- Data ‘1’ level: 1.06V
- Data ‘0’ level: 0.43V

**Proposed 2T1C**

- 65nm LP, 1.1V, 85°C
- Data ‘1’ level: 0.76V
- Data ‘0’ level: 0.28V

1. Low data ‘1’ level
2. Data ‘0’ write-back
3. Narrow window between ‘1’ and ‘0’

1. Beneficial couple-up during read (PC)
2. Preferential couple-down during write-back (PC)
3. Circuit techniques to enhance retention time
   1) Repair scheme utilizing single-ended 7T SRAM
   2) Storage monitor for PVT-aware refresh control
Read and Write-back Timing

- A 0.2V beneficial couple-up read and a 0.28V preferential couple-down write-back

Single-ended 7T SRAM Repair Cell

- Decoupled read and local differential write
- Shares control signals (WL’s and BL’s) with the 2T1C array allowing seamless integration
Tail Cell Repair Scheme

- 1-BL repair case with a target retention of 500µs
  - 2T1C repair: 6.25% failure (left)
  - 7T SRAM repair: No failure with 1.2% (4.8%) array overhead at 1-repair BL per 128 BL’s (32 BL’s)
Storage Voltage Monitor

- Storage voltage monitor with varying retention time and under PVT variations
  - Gain cell specific retention sensor including leakages and coupling effects for PVT-aware refresh control
**EDRAM Test Chip Microphotograph**

- **Process**: 65nm LP CMOS
- **Ckt dimension**: 556x345µm²
- **Array size**: 2x64kbits (Conv. 3T & Prop. 2T1C)
- **Cell size**: 58% of 6T SRAM
- **Retention time**: 500µs @ 1.1V, 85°C
- **Random cycle time**: 1.40ns (714MHz) @ 1.1V
- **VMIN**: 0.7V @ 10µs retention
- ***Refresh power**: 161.8µW per Mb (**0.28X of 6T SRAM**)

- **714MHz random cycle at a 500µsec retention time with 1-BL repair per 32 BL’s**
- **72% lower data retention power compared with a power-gated 6T SRAM**
- The proposed 2T1C gain cell achieves practical retention time (>100µs) with no boosted supplies
Measured VDD Shmoo

- Wide operating voltage range of 0.7V ~ 1.4V (left)
- 72% smaller refresh current than SRAM leakage at a power-down retention voltage of 0.6V (right)
Summary

• Gain cell eDRAM contender for future e-memory
  – Logic-compatible, decoupled read and write paths
  – 2X bit cell density, 0.3X static current than SRAM

• A fully logic-compatible eDRAM proposed
  – 2T1C gain cell with no boosted supplies
  – Single-ended 7T SRAM repair scheme
  – Storage monitor for PVT-aware refresh control

• A 1.1V, 65nm 64kb eDRAM chip demonstrated
  – DRAM implementation based on only thin $T_{\text{OX}}$ devices
  – 1.4ns cycle time at a retention time of 500µs at 85°C
  – 161.8µW per Mbit static power dissipation at 85°C
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