A Switched Decoupling Capacitor Circuit for On-Chip Supply Resonance Damping

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Outline

• Introduction to resonant supply noise
• Proposed switched decap circuit
• Simulated supply noise suppression
• Test chip implementation
• Supply noise measurement results
• Conclusion
IC Power Supply: Underdamped RLC Network

On-Chip Power Grid

- Resonant noise exhibits large magnitude and long duration
- Causes timing violation, clock skew and reliability issue
- Excited by μP loop operation or sudden current spike

N. Na, IBM, ECTC 2004
Previous Passive Damping Techniques

- Increase R and C to bring down the Q factor
- Decap consumes large area and gate leakage
- Resistive damping worsens IR drop

\[ Q = \frac{1}{R_{\text{wire}}} \sqrt{\frac{L}{C}} \]

Previous Active Damping Techniques

- Detect resonant noise and clamp the overshoot
- 1mA static current per 3mA load
- Hard to control trip points under PVT variation
- Only compensates voltage overshoot

J. Xu et al., Intel, ISSCC 2007
Previous Active Damping Techniques

- Switching decaps to boost the total charge
- 5mA quiescent current per regulator
- Limited swing and PVT sensitivity in opamp

M. Ang et al., Sun Microsystems, ISSCC 2000
Principle of Switched Decap Circuit

- \( Q_{\text{swdecap}} = 0.5C \cdot V_{dd} + C \cdot \Delta V_{dd}/2 \)
- \( Q_{\text{pdecap}} = 2C \cdot \Delta V_{dd} \)
- 5–13X charge boosting factor (i.e. \( Q_{\text{swdecap}}/Q_{\text{pdecap}} \))
**Proposed Digital Switched Decap**

- Digital resonant detection circuit
  - Simple implementation for digital ICs
  - Low static power
- Programmable $V_{SW}$, PVT insensitive design
Bandpass and PVT Insensitive Design

• RC circuit & delay line realize bandpass filter
• 8mV worst-case $V_{SW}$ variation
Adjustability of Switching Threshold $V_{SW}$

- $V_{SW}$ can be adjusted to avoid unnecessary switching
- $V_{SW}$ is approximately proportional to $R$ value
- $R$ implemented using a programmable MOSFET array

![Graph showing the relationship between $V_{SW}$ and $R$](image)
Simulated Switched Decap Performance

- Resonance is suppressed by 7dB
- More than 8X decap boost for resonant damping
Simulated First-droop Regulation

- Both magnitude and oscillation time are reduced for first-droop noise
- 6X+ decap boost compared with passive decap
Test Chip Organization

- Two types of noise generation circuits
- Selection of swdecap value: 100pF, 200pF, 300pF
- On-chip sensor to measure differential noise
Resonance Generation Logic

- Creates harmonics at resonant frequency
Supply Noise Measurements

- 640MHz clock gated by 1/16
- 5.5dB noise reduction using 200pF swdecap
- $f_{res}$ at 40MHz lower than expected due to package inductance
Frequency Domain Measurements

- 9.8dB suppression using 300pF swdecap
- No significant impact on non-resonant frequency noise
• Noise magnitude more sensitive to swdecap value than $V_{SW}$
Comparison with Passive Damping

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<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>100pF</td>
<td>2.2dB</td>
<td>500pF</td>
<td>5X</td>
<td>0.1Ω</td>
</tr>
<tr>
<td>200pF</td>
<td>5.5dB</td>
<td>1500pF</td>
<td>7.5X</td>
<td>0.4Ω</td>
</tr>
<tr>
<td>300pF</td>
<td>9.8dB</td>
<td>3500pF</td>
<td>11X</td>
<td>1Ω</td>
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- 5–11X boost over passive decaps
- Equivalent to 0.1-1Ω resistive damping
- Passive resistor aggravates IR drop
## Performance Comparison

<table>
<thead>
<tr>
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<th>Active Damping Ckt.*</th>
<th>This work</th>
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<tbody>
<tr>
<td><strong>Technology</strong></td>
<td>90nm</td>
<td>130nm</td>
</tr>
<tr>
<td><strong>Static Current</strong></td>
<td>2.42mA</td>
<td>0.54mA</td>
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<tr>
<td><strong>Load Current</strong></td>
<td>8.71mA (3X $I_{static}$)</td>
<td>33mA (61X $I_{static}$)</td>
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<tr>
<td><strong>Regulator Area</strong></td>
<td>59x20μm$^2$</td>
<td>190x220μm$^2$ (including 300pF)</td>
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<tr>
<td><strong>First Droop</strong></td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Regulation</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Analog Opamp</strong></td>
<td>Yes</td>
<td>No</td>
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* J. Xu et al., Intel, ISSCC 2007
Die Photograph and Chip Summary

- 9X less static current compared with prev. swdecap design
- Swdecap serves as passive decap under norm. condition
- Up to 11X decap boost compared with passive decap
- Negligible power consumed for decap switching (1.2%)

**Technology**
- 0.13μm Logic CMOS

**Quiescent Current**
- 0.54mA

**Regulation Frequency**
- 10–300MHz

**Regulator Area (w/o decap)**
- 100μmx70μm

**Regulator Area (w/ 300pF decap)**
- 190μmx220μm

**Total Die Area**
- 0.9mx1.8mm
Conclusions

• Resonant supply noise impacts circuit performance and reliability

• A switched decap circuit is proposed
  – Low power resonant detection circuit
  – Digital-friendly implementation
  – Programmable and PVT insensitive switching threshold

• 0.13μm test chip implemented
  – 5–11X boost in effective decap value
  – Up to 9.8dB resonant noise suppression
  – 9X reduction in static current compared with previous switched decap design