Measurement, Analysis and Improvement of Supply Noise in 3D ICs

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Abstract

Supply noise measurements from a 3D IC have been presented for the first time. IR noise rather than Ldi/dt noise is shown to be dominant due to the fewer supply pins and the additional resistance from the through-silicon vias (TSVs). Kelvin probing for IR noise reveals that the effect of pins is significantly more than TSVs. A novel multi-story power delivery is demonstrated for a 393kb SRAM suppressing the IR noise by 30-70%.

Introduction

Power delivery challenges are exacerbated in 3-dimensional integrated circuits (3D ICs) due to the large supply currents that need to reach to the bottom tier in a stacked die, passing through long resistive TSVs. In addition, the reduced footprint of the chip leads to a smaller number of IO pads that can be used for power supplies compared to 2D. The resulted increased IR and Ldi/dt noise may cause a larger variation in operating speed leading to more timing violations. The supply noise behavior would also be different across individual tiers. For example, the shielding impact of the adjacent tiers on each other can alter the Ldi/dt noise, or there can be increased damping due to extra resistive parasitics. Despite the severity of the problem, research on 3D IC power delivery has mainly been limited to modeling and architectural studies without verification from silicon [1][2]. In this work, we present power supply noise measurements and mitigation techniques from a 3D IC test chip vehicle built in a 1.5V, 150nm, 3-tier, fully depleted silicon-on-insulator process from MIT Lincoln Labs. The process used in this technology is a via-first approach leading to a configuration in Fig. 1. The top, mid and bottom tiers are referred respectively as *t*, *m*, and *b*. The *t* and *m* tiers are face to back (*f2b*) while the *m* and *b* are face to face (*f2f*).

TSV Characterization

In order to fully understand and model the impact of TSVs on the supply noise of 3D ICs, accurate characterization of the TSV parasitics must precede. Fig. 2 shows a simple daisy chain structure used in the test chip to obtain TSV resistance for different pair of tiers. The resistance of the stacked *t-b* TSV is slightly more than the sum of the resistances for *t-m* and *m-b* cases, which follows from the geometry of the TSV and different layers. There was no noticeable difference in the TSV resistance between the *t-m* and *m-b* layers. The performance impact of TSV capacitance on digital circuits is evaluated by a 3D ROSC array test setup in Fig. 3. It consists of sets of 9 inter-tier communicating ROSCs. They connect between *t-m, m-b* and *t-b* tiers each with intermittent TSV connection every 1, 2 or 4 inverters, with 5, 10 or 20µm TSV pitches, respectively. The divided frequency output of the selected ROSC module is read off chip. Fig. 4 makes a comparison of 2D ROSCs in *t*, *m* and *b* tiers, and, *t-b* 3D ROSC with TSVs every 1, 2 and 4 inverters. In this 3D IC process, *t* is significantly faster, while the ROSC performances in *m* and *b* are almost identical. The TSV loading can affect the ROSC frequency as much as 38% for the 1 inverter per TSV case. In order to cancel out the effect of the large inter-tier process variation, results were normalized against a no TSV case for that pair of tiers. Fig. 4 (right) show the normalized ROSC periods of the TSV loaded ROSCs. Numerically, it plots $N_{TSV}C_{TSV}R_{INV}/C_{INV}R_{INV}$. While, the *t-m* and *m-b* TSVs behave similarly, the *t-b* TSV is not simply a sum of former two. The lower figure plots the estimated C_{TSV}/C_{INV}, which is 40-60% and includes inter-TSV coupling.

Supply Noise Measurement

In order to capture the supply noise behavior across different tiers in a 3D IC, the test setup in Fig. 5 was constructed. It consists of noise sensing (*Nsen*) and generation (*Ngen*) modules in each tier. 80 TSVs for the noisy supply DVDD were put at a pitch of 5µm occupying an area of ~2500µm^2. The *Ngen* module consists of a programmable number of units, each consisting of a clock gated switch to control the current drawn from DVDD. A VCO sweeps the clock frequency. The *Nsen* differentially captures the AC noise between DVDD and DGND in frequencies ranging from 1MHz to 500MHz with a gain of 10dB [3]. We first capture the noise spectrum in different tiers of a 3D IC by providing current excitation to that tier. From Fig. 6 (left), *t* shows a resonant peak while the peak noise in other two tiers is markedly reduced, -53% for *b* and -72% for *m*. This reveals significant shielding effect from tiers *t* and *b* on tier *m*. In addition, the TSVs provide decap as well as resistive damping, although those would be second order effects based on the characterized values.

Next we compare the noise spectrum of the top tier *t* with that of a 2D circuit. From Fig. 6 (right), there is no significant difference in the peak noise amplitude. The higher frequency noise amplitude is also same. However, there is a shift in the resonant frequency owing to a lesser inductance with the fewer pads. Measurements indicate that the AC noise problem is largely unaffected from the 2D case for tier *t*. IR noise on the other hand, is directly affected by the reduced pads and the TSVs in the supply path. Fig. 7 shows the comparison between 2D and 3D (tier *b*). For a 100mV supply drop, the I_{MAX} is 69% less in 3D. For the test setup, most of the supply drop contribution is due to the 3X fewer pads available as seen in Fig. 7. The contribution of TSVs to the supply drop in each tier can also be seen in Fig. 7. The *t-m* path has more TSV drop than the *m-b* path owing to the *f2b* arrangement in the former versus *f2f* in the latter. Projections can be made off this measured data to obtain the required TSVs and pads for achieving a particular I_{MAX}. For example, for a 7A current, 400 TSVs and 125 pads would be required for less than a 100mV IR drop.

Multi-Story Power Delivery for 3D ICs

The above results indicate that IR noise is a severe problem for 3D ICs much more than the 2D case. A novel concept based on current recycling between logic blocks has been proposed as an efficient DC-DC converter as well as reducing supply noise [4]. Fig. 8 illustrates the concept. If the currents are exactly balanced in the upper and lower "stories", the middle supply node is "quiet", leading to reduction in both IR and Ldi/dt noise. The idea can be readily extended to 3D ICs in what we call the 3D multi-story power delivery (3D-MSPD) scheme. The inherent split configuration of a 3D IC makes splitting of supplies and hence implementation of MSPD more efficient than in conventional 2D ICs where the partitioning of circuit blocks can be tricky. A simple circuit model for MSPD is derived from a conventional 3D IC model in Fig. 9 (top). The worst case IR noise occurs when one of the stories is completely off as the imbalanced currents will lead to a larger supply noise in the middle supply node. Measured data shown for a 3D-MSPD scheme in Fig. 9 (bottom) reveals a 1.4-2.8x boost in I_{MAX}. A 393kb SRAM was implemented to demonstrate the 3D-MSPD technique. All external input and output signals are in the VDD-Gnd domain, while the internal ones are level up converted to the 2VDD-VDD domain. A capacitive coupling based level up/down converters were used for signal translation between these two domains. Fig. 10 summarizes the results and shows the microphotograph image of the test chip.

Acknowledgements

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References

[1] N. Khan et al., TVLSI, 2009 [2] G. Huang et al., EPEP pp. 205-208 , 2007 [3] J. Gu et al., VLSI Circuits Symp., pp. 126-127, 2007 [4] S. Rajapandian, et al., ISSCC, pp. 298-299, 2005

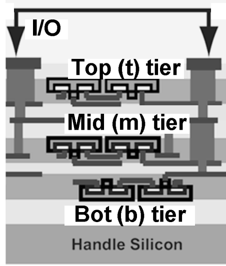

Fig. 1. Cross section of 3D IC FD-SOI technology.

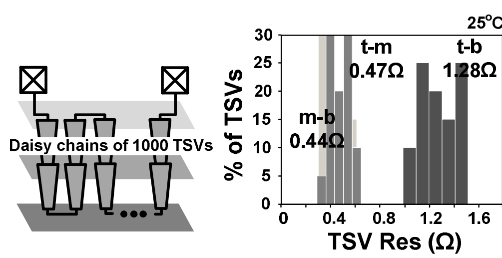

Fig. 2. Test structure for measuring TSV resistance (left). Measured TSV resistance distribution (right).

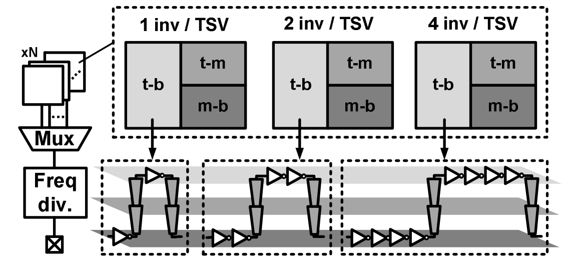

Fig. 3. Test setup to obtain TSV capacitance and effect on ROSC frequency

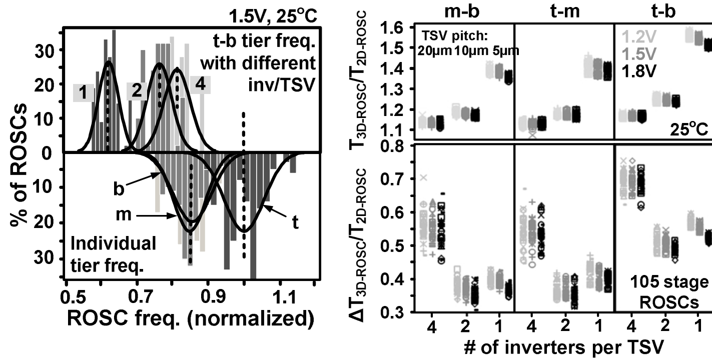

Fig. 4. Measured 3D-ROSC frequencies and inter-tier variation (left). Effective TSV loading on 3D-ROSCs (right).

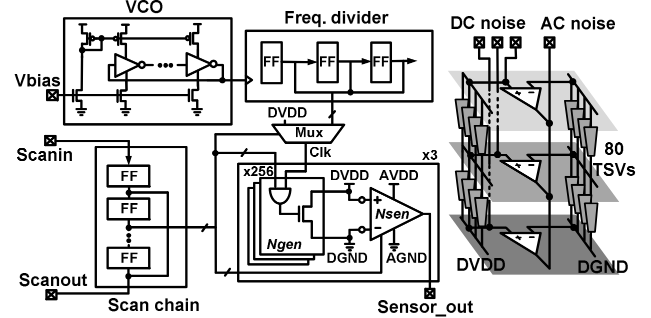

Fig. 5. DC and AC supply noise measurement setup.

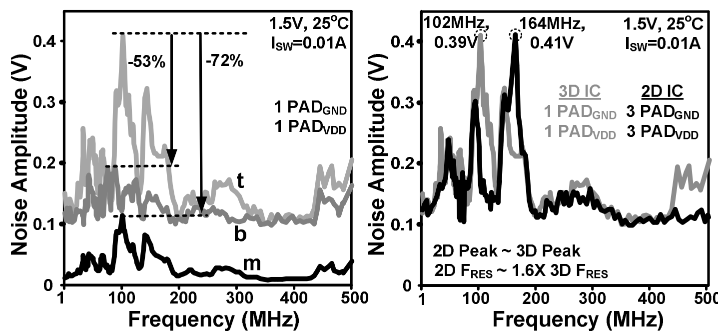

Fig. 6. Measured AC noise in different tiers (left) and between 3D and 2D configurations (right).

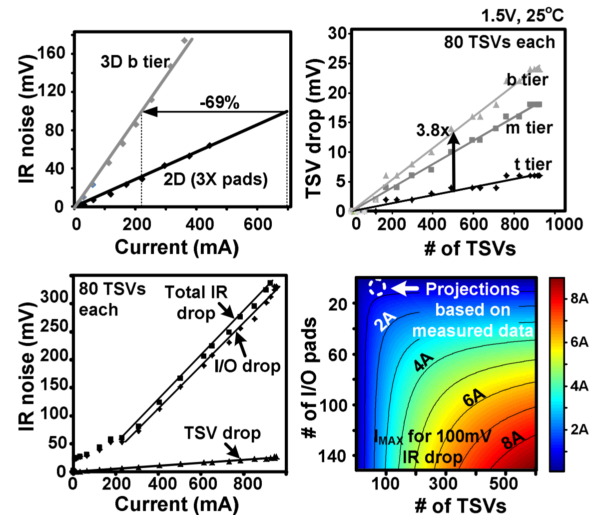

Fig. 7. 2D vs. 3D IR noise and division of IR drop between pads and TSVs (left). IR noise between different tiers and I_{MAX} dependencies on pad and TSV counts (right).

Technology	150nm FD-SOI	F_{max} and power	470MHz,10.7mA @ 1.5V, 25°C
Chip dim.	4mm x 4mm	Area overhead	7%
SRAM size	393kb, 6T cell	Performance overhead	15%
SRAM area	2.1mm x1.9mm		

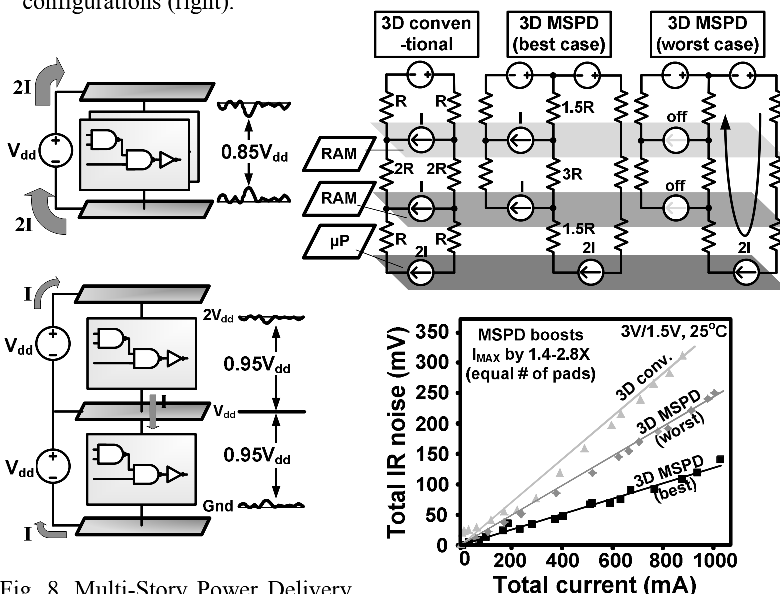

Fig. 8. Multi-Story Power Delivery (MSPD) technique for supply noise reduction in 2D and 3D ICs.

Fig. 9. Conv. and proposed MSPD schemes for 3D ICs (top). Measured supply noise comparison (bottom).

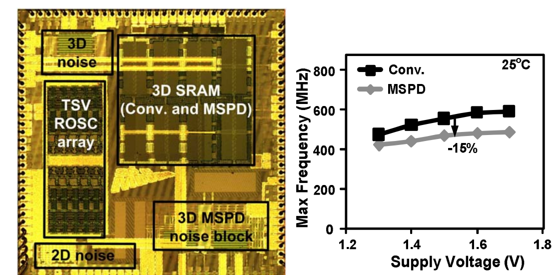

Fig. 10. 3D-MSPD SRAM measurement summary (top). Die microphotograph (lower left). Performance comparison of conv. 3D and 3D-MSPD SRAM (lower right).