A 32nm, 0.9V Supply-Noise Sensitivity Tracking PLL for Improved Clock Data Compensation Featuring a Deep Trench Capacitor Based Loop Filter

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Outline

• Resonant Supply Noise Issue
• Introduction to Clock Data Compensation
• Proposed 32nm Supply-Noise Tracking PLL
• Deep Trench Capacitor Based Loop Filter
• PLL Test Chip Measured Data
• Summary
Resonant Supply Noise Basics

- Resonance between package/bonding inductance and on-die decoupling capacitance
- Typical resonant frequency: 40-300 MHz
- Typical resonant noise amplitude: ~10%

[1] N. Kurd et al., JSSC 2009
Clock Data Compensation (CDC)

- Clock period modulated by resonant noise
- Performance loss partially alleviated by intrinsic CDC
- Optimal CDC: Make CLKo period track datapath delay
Techniques for Enhancing CDC

- Key control parameters: Clockpath supply, PLL output clock (CLKi) period
Adaptive PLL achieves optimal CDC by modulating the CLKi period using the supply noise.
Existing PLLs for Enhancing CDC

- Prior works: open-loop, one-time programmable
- Proposed work: closed-loop, real-time PVT tracking

[1] N. Kurd et al., JSSC 2009
Clockpath and Datapath Timing Models

- Datapath delay: Proportional to supply voltage
- Clockpath delay: Must account for the delay difference between two consecutive clock edges
By making $A = B$ using an adaptive PLL, the $CLK_o$ period becomes independent of $D(t)$ and is perfectly aligned with the datapath delay, leading to an optimal CDC condition.

$$CLK_o \text{ period} = A \sin(t-D) + B \sin(t) - B \sin(t-D)$$

$$= B \sin(t) \quad \text{when} \ A = B$$

- By making $A = B$ using an adaptive PLL, the $CLK_o$ period becomes independent of $D(t)$.
- The $CLK_o$ period is perfectly aligned with the datapath delay, leading to optimal CDC.
Comparison with Prior Art

<table>
<thead>
<tr>
<th></th>
<th># of control parameters</th>
<th>Parameter setting</th>
<th>Passive area</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conv.</td>
<td>None</td>
<td>None</td>
<td>Large</td>
</tr>
<tr>
<td>[1]</td>
<td>One (sensitivity)</td>
<td>1D sweep, one time</td>
<td>Large</td>
</tr>
<tr>
<td>[2]</td>
<td>Two (phase, sensitivity)</td>
<td>2D sweep, one time</td>
<td>Large</td>
</tr>
<tr>
<td>This work</td>
<td>*One (sensitivity)</td>
<td>Closed-loop tracking</td>
<td>Small ($C_{trench}$)</td>
</tr>
</tbody>
</table>

*Key requirement for stable closed-loop tracking
Effectiveness of PVT Tracking

- Conv. PLL
- Fixed Sensitivity
- Optimal Sensitivity

32nm, 0.9V HKMG SOI (Sim. & Measured)

Normalized $F_{\text{max}}$ (%)

- Nominal
- SS $-20\%V_{\text{dd}}$, $120^\circ\text{C}$
- FF $+20\%V_{\text{dd}}$, $20^\circ\text{C}$
- (Meas.) $-20\%V_{\text{dd}}$, $120^\circ\text{C}$
- (Meas.) $+20\%V_{\text{dd}}$, $20^\circ\text{C}$
Proposed Supply-Noise Tracking PLL

- CDC Modulator
- Tunable Critical Path Bit Error Monitor
- Supply-Noise Sensitivity Tracking Control
- Charge-Pump PLL
- Clockpath
Conventional CP PLL & Clockpath
Supply-Noise Sensitivity Tracking Loop

slide 13
CDC Modulator & Tunable ERR Monitor

Sensitivity = \( \frac{C_d}{C_u + C_d} \) 

\[ \text{VDD} \]

\[ C_u \rightarrow \text{C} \rightarrow \text{C} \rightarrow \cdots \]

\[ \text{EN}[0] \rightarrow \text{EN}[1] \rightarrow \text{VBN} \rightarrow \text{EN}[62] \]

\[ C_d \rightarrow \text{C} \rightarrow \text{C} \rightarrow \cdots \]

\[ \text{RST} \rightarrow \text{CLKo} \rightarrow \text{Datapath} \rightarrow \text{CLKo} \]

\[ \text{CDC modulator} \rightarrow \text{Binary to therm.} \rightarrow \text{Counter} \rightarrow \text{Digital filter} \rightarrow \text{Tunable critical path bit error monitor} \]

\[ \text{Ref. CLK} \rightarrow \text{PFD} \rightarrow \text{UP} \rightarrow \text{DN} \rightarrow \text{CP} \rightarrow \text{LF} \rightarrow \text{VCO bias gen.} \rightarrow \text{Diff. VCO} \rightarrow \text{MUX} \]

\[ \text{Various clockpaths} \rightarrow \text{Digital supply: VDD} \]
Tracking Loop Transient Response

VDD noise example

BER info

Counter output
- BER tracking operation

PLL output clock period

Before ASST locking
- PLL control voltage (VBN)
- VDD first-droop noise

After ASST locking
Deep Trench Capacitor

- Vertical shape $\rightarrow$ ~50x higher density than thick-oxide
- Applications: eDRAM, decoupling cap., DC-DC
- Drawbacks: additional cost, high internal series res.

G. Wang et al., IEDM 2009
Deep Trench Cap. Based Loop Filter

- Dense deep trench cap. used for PLL’s integrating cap. for the first time → area reduction
- Thick-oxide cap. used as a ripple reject cap. → no phase noise degradation

<table>
<thead>
<tr>
<th>C_i</th>
<th>C_p</th>
<th>Area</th>
<th>Ripple Noise</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thick Oxide</td>
<td>Thick Oxide</td>
<td>☹</td>
<td>😊</td>
<td>Large area due to thick oxide C_i</td>
</tr>
<tr>
<td>Thin Oxide</td>
<td>Thin Oxide</td>
<td>😊</td>
<td>☹</td>
<td>Large ripple due to gate leakage</td>
</tr>
<tr>
<td>Deep Trench</td>
<td>Deep Trench</td>
<td>😊</td>
<td>☹</td>
<td>Large ripple due to trench cap series res.</td>
</tr>
<tr>
<td>Deep Trench</td>
<td>Thick Oxide</td>
<td>😊</td>
<td>😊</td>
<td>Compact area and minimal ripple</td>
</tr>
</tbody>
</table>

N. Butt et al., IEDM 2010
Measured $F_{\text{max}}$ with Capacitor Types

- Deep trench vs. thick oxide integrating capacitor
- No noticeable difference in PLL performance
Area Reduction with Deep Trench Cap.

- Capacitor area ratio = 0.00115mm² / 0.0648mm² = 1/56
Die Photo and Performance Summary

<table>
<thead>
<tr>
<th>Process</th>
<th>32nm HKMG SOI</th>
<th>Deep trench PLL area</th>
<th>0.0055mm²</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>0.9V</td>
<td>Conv. PLL area</td>
<td>0.0692mm²</td>
</tr>
<tr>
<td>$F_{\text{max}}$ improvement (w/ 90mV noise)</td>
<td>14.5%~15.6%</td>
<td>PLL area reduction</td>
<td>*-92.1% **-43.6%</td>
</tr>
</tbody>
</table>

Compared to *single-path PLL and **dual-path PLL with 12:1 ratio
**Measured $F_{\text{max}}$ vs. Noise Amplitude**

32nm, 0.9V, room temp.

- **14.5% ~ 15.6%** $F_{\text{max}}$ improvement for 90mV noise amplitude @ 100MHz
- $F_{\text{max}}$ improvement proportional to noise amplitude

**Clockpath Config.**
- Red: No interconnect
- Green: Short interconnect
- Blue: Medium interconnect
- Purple: Long interconnect
Measured $F_{\text{max}}$ vs. Noise Frequency

- 9.9% ~ 14.2% $F_{\text{max}}$ improvement for 40~320MHz
- Proposed PLL effective across a wide frequency range
Summary

• Resonant supply noise is a growing concern in low voltage processors

• Existing PLL designs for enhancing CDC involve exhaustive search of key tuning parameters

• Proposed 32nm sensitivity-tracking PLL
  – Timing-model based approach to optimize CDC
  – Automatic supply-noise sensitivity tracking loop
  – Low-area deep trench capacitor based loop filter
  – $15\% F_{\text{max}}$ improvement, 92.1% PLL area reduction